上海交通大学
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Lecture 11

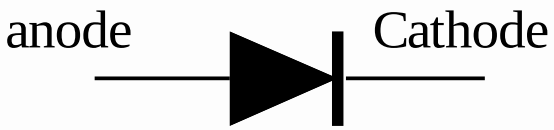
Diodes

- Diode:
- ✓ The simplest and most fundamental nonlinear circuit element.
- ✓ Used as the generation of dc voltages from the ac power supply.
- ✓ Foundation for understanding the characteristics of bipolar transistors and the field-effect transistors.
- Silicon pn-junction diodes .
- Specialized diodes types:

  photodiode

  the light-emitting diode.

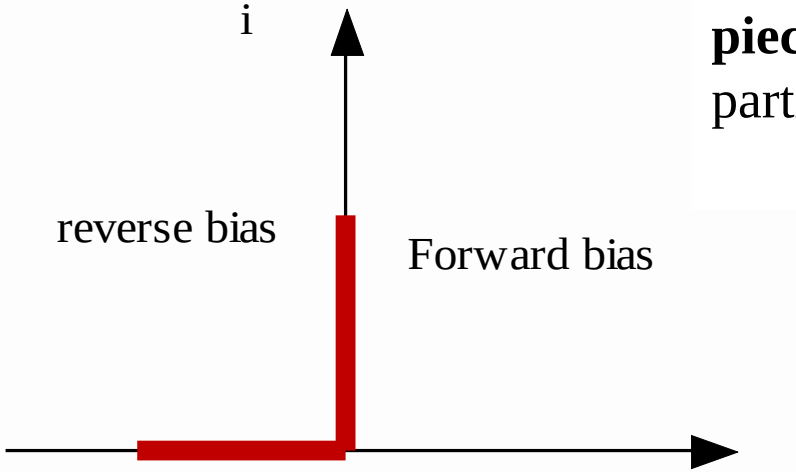
1. Ideal diode



diode circuit symbol

Nonlinear characteristics:
1. cutoff state: When the diode is reverse-biased , it behaves as an open circuit.
2. On state: when the diode is forward-biased, it behaves as an short circuit.

i-v curve includes two straight line, so it is **piecewise linear** . The diode is a linear circuit in a particular operation region.

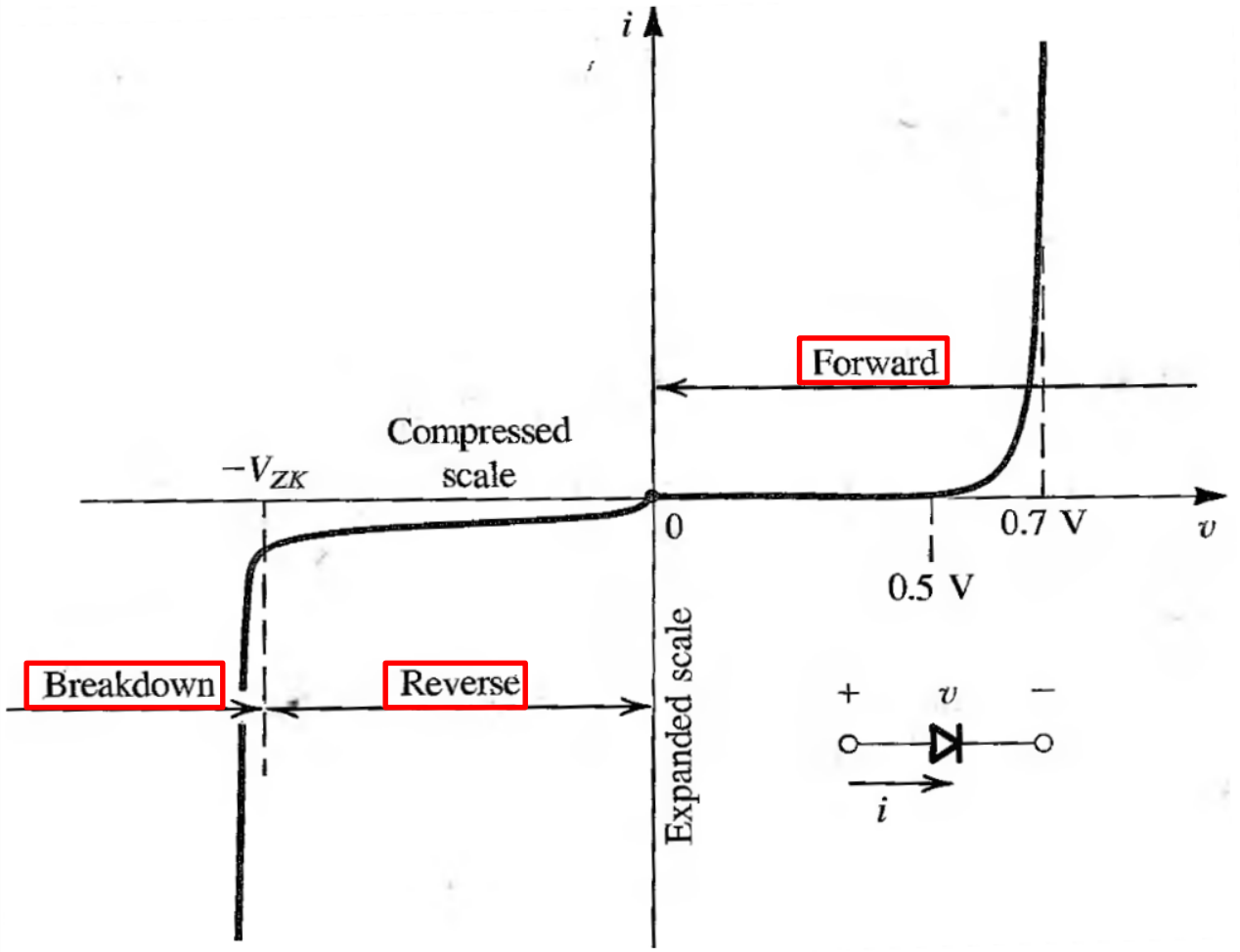


i-v curve

Diode application
1. The **rectifier** converts ac voltage to dc voltage.
2. Diode logic gate: such as “OR” gate and “AND” gate.

2 Terminal characteristics of junction diodes

I-V relationship



$$i = I_S(e^{v/nV_T} - 1)$$

I_S: **saturation current** ,constant for a given temperature and pn junction.

n: constant of value between 1 and 2, depending on material and structure of diode.

n=1 for integrated circuit fabrication process

n=2 for discrete diodes.

Thermal voltage : $V_T = \frac{kT}{q}$

K= Boltzmann's constant=1.38×10^{-23} joules/Kelvin

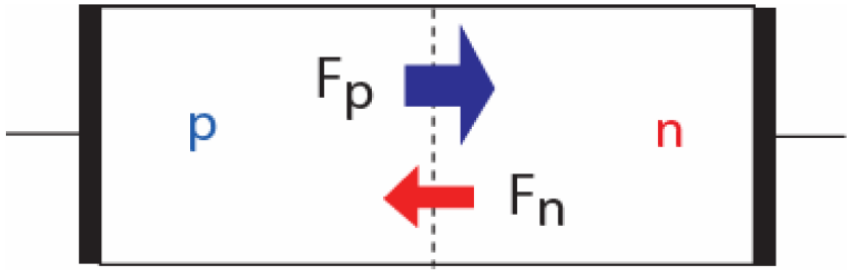
T= the absolute temperature in kelvins=273+temperature in Centigrade

q= the magnitude of electronic charge= 1.60×10^{-19} coulomb in room temperature ($25^{\circ}C$)

Cut-in voltage: the current is very small if the voltage is smaller than 0.5V.

Physics of forward bias:

Diode Current equation: $I_D = I_0[\exp(\frac{qV_D}{kT}) - 1]$

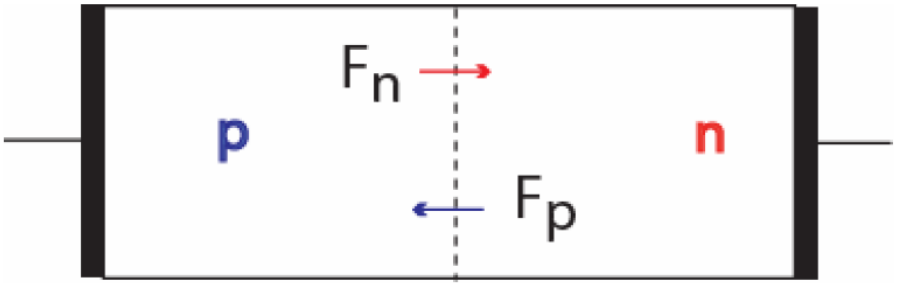


- Junction potential φ_J (potential drop across SCR) reduced by $V_D \Rightarrow$ **minority carrier injection into QNRs**
- Minority carrier diffusion through QNRs
- Minority carrier recombination at contacts to the QNRs (and surfaces)
- Large supply of carriers injected into the QNRs

$$\Rightarrow I_D \propto [\exp(\frac{qV_D}{kT})]$$

Physics of reverse bias:

$$I_D = I_0[\exp(\frac{qV_D}{kT}) - 1]$$



- Junction potential φ_J (potential drop across SCR) increased by $|V_D|$ $\Rightarrow$ **minority carrier extraction from QNRs**
- Minority carrier drift through QNRs
- Minority carrier generation at surfaces & contacts of QNRs
- Very small supply of carriers available for Extraction $\Rightarrow$ I saturates to small value

$$\Rightarrow I_D \approx -I_0$$

The pn junction in the breakdown region

- When the reverse voltage exceeds the breakdown voltage, the diode is breakdown. Or if the reverse current *I* is greater than the drift current *Is*, breakdown occurs.
- The two possible breakdown mechanisms :

  zener effect （齐纳效应）

  avalanche effect. （雪崩效应）
- pn junction breakdown is not a destructive process, provided that the maximum specified power dissipation is not exceeded.

3. Analysis of diode circuits

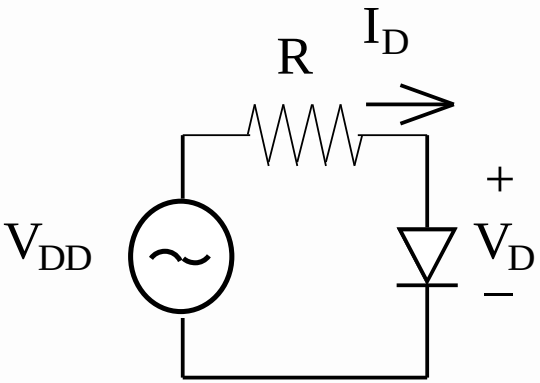


Fig. a simple diode circuit

We can represent the diode *I*-*V* characteristic by the exponential relationship, resulting in

$$I_D = I_S e^{V_D / nV_T}$$

The other equation is obtained by writing a Kirchhoff loop equation, resulting in

$$I_D = \frac{V_{DD} - V_D}{R}$$

I_D and V_D can be obtained by two solutions: **graphical analysis** and **iterative analysis**.

Graphical analysis

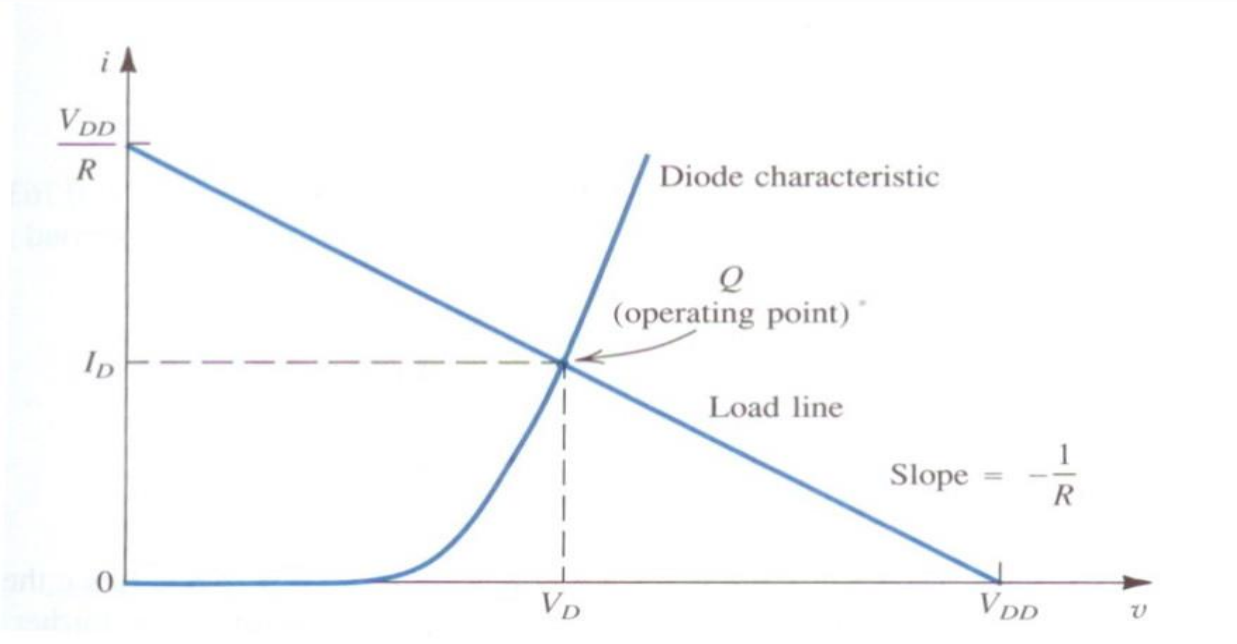


Fig11.1 Graphical analysis of the simple diode circuit

The operation point is the intersect of the diode curve and the load line. Its coordinates give the values of I_D and V_D.

Iterative analysis

1) Assume I_D and V_D to be the V_1 and I_1

2) Substitute V_1 into $I_D = \frac{V_{DD} - V_D}{R}$ to get I_2

3) Substitute V_1 I_1 and I_2 into $V_2 - V_1 = 2.3nV_T \log \frac{I_2}{I_1}$

to get V_2

4) Make iterative computation like 2) and 3),

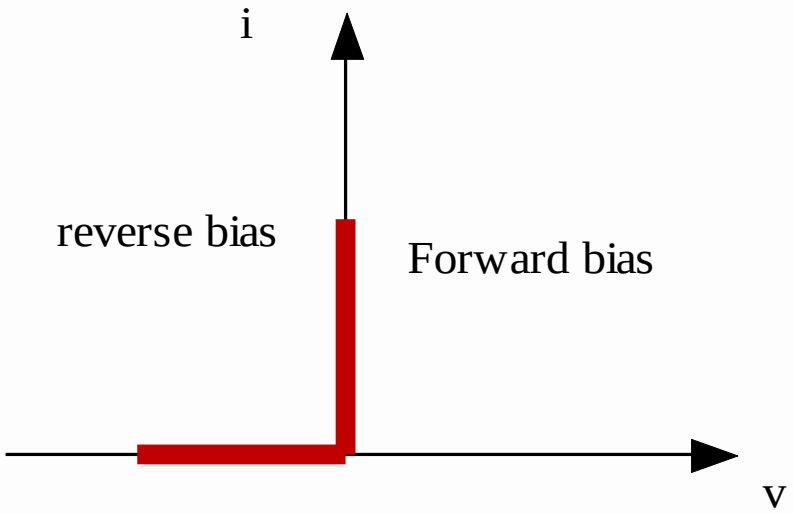
until $V_n - V_{n-1} <$ convergent limit

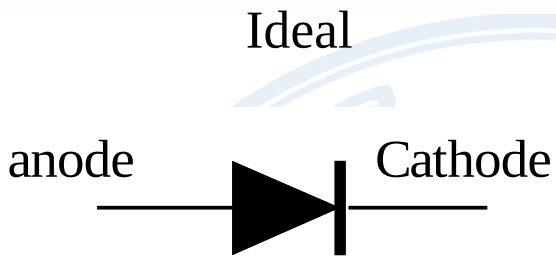
iteration stops. I_n and V_n are I_D and V_D, respectively.

4. Diode circuit models

- Large-Signal Static Model
  1) Ideal model
  2) The constant-voltage drop model
  3) Piece-wise linear model
- Small Signal Model
  1) Small signal resistance
  2) Depletion capacitance and junction capacitance

Ideal model





The constant-voltage drop model

The model simply says that a forward-conducting diode exhibits a constant voltage drop V_D of value usually taken to be *0.7V*. This model is usually employed in the initial phase of analysis and design.

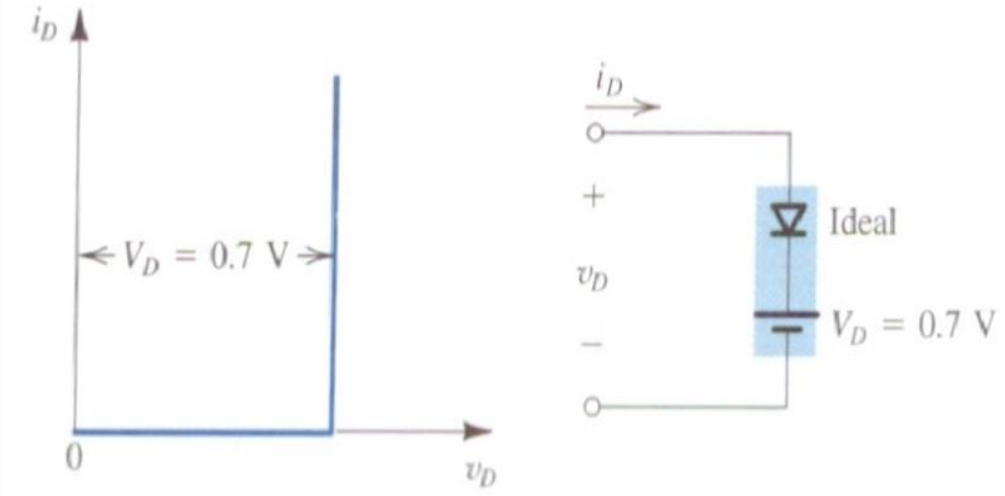


Fig The constant voltage drop model and its circuit representation

Piece-wise linear model

The nonlinear nature complicates the analysis of diode circuits. For simplification, the exponential curve is approximated by two straight lines.

$$i_D = 0, \quad v_D \le V_{D0}$$

$$i_D = (v_D - V_{D0}) / r_D, \quad v_D \ge V_{D0}$$

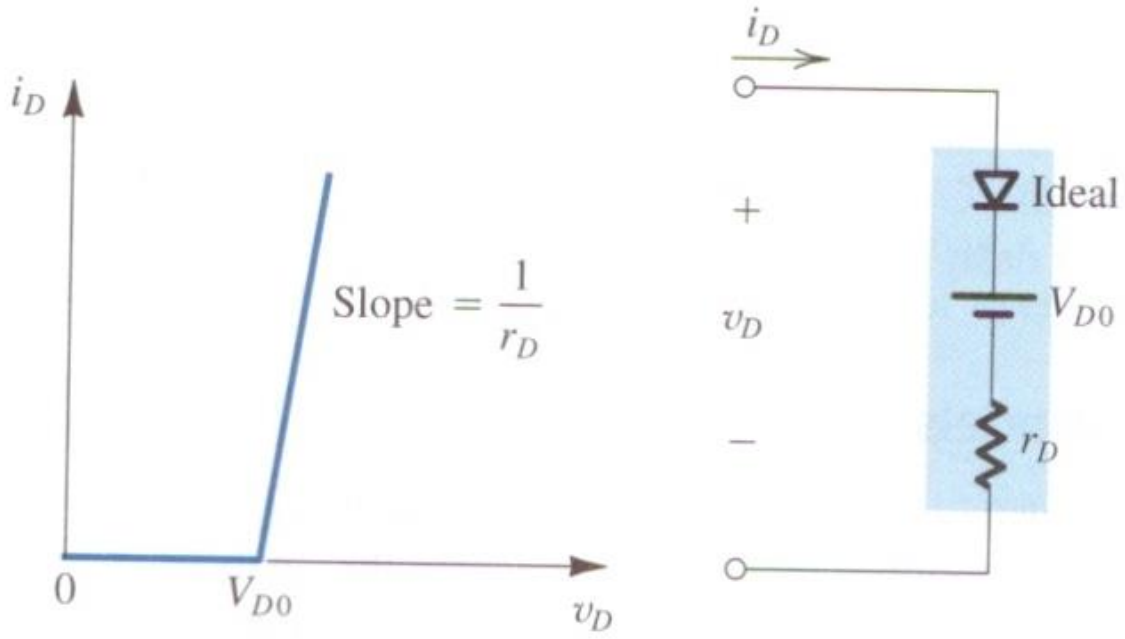


Fig Piecewise-linear model of the diode forward characteristics and its equivalent circuit representation

Question?

How does a circuit designer to select various models?

This selection is a compromise between accuracy and complexity for specific application.

The small signal model and its application

- Nonlinear system to linear system- Small signal resistance
- When a diode is biased to operate at a point on the forward *I*-*V* characteristic and a small ac signal is superimposed on the dc quantities, the diode is best modeled by a resistance equal to the inverse of the slope of the tangent to *I*-*V* characteristic at the bias point. This model is called diode small signal model.

First, we decompose the total voltage v_D across the forward biased diode into a DC voltage V_D and an incremental voltage v_d, that is, defined by

$$v_D = V_D + v_d$$

Examine effect of small signal overlapping bias:

$$i_D = I_D + i_d = I_0[\exp(\frac{q(V_D + v_d)}{kT}) - 1]$$

If the amplitude of the signal $v_d(t)$ is kept sufficiently small such that

$$\frac{v_d}{kV_T} << 1$$

We may expand the exponential in a series and truncate the series after the first two terms to make small-signal approximation.

$$I_D + i_d = I_0[\exp(\frac{qV_D}{kT})\exp(\frac{qv_d}{kT}) - 1]$$

$$\approx I_0[\exp(\frac{qV_D}{kT})(1 + \frac{qv_d}{kT}) - 1]$$

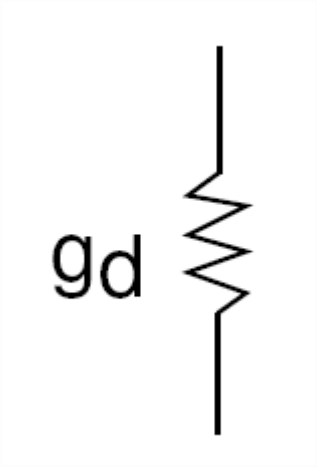
$$= I_0[\exp(\frac{qV_D}{kT}) - 1] + I_0 \exp(\frac{qV_D}{kT})(\frac{qv_d}{kT})$$

$$i_d = \frac{q(I_D + I_0)}{kT} v_d$$

The total current= the dc current +the ac current (small signal)

$$i_D(t) = I_D + i_d$$

From a small signal point of view. Diode behaves as **conductance of value:**



$$g_d = \frac{q(I_D + I_0)}{kT} \approx \frac{qI_D}{kT}$$

g_d depends on bias.

In forward bias:

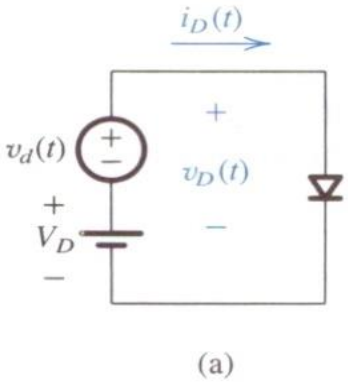
$$g_d = \frac{qI_D}{kT}$$

g_d is linear in diode current.

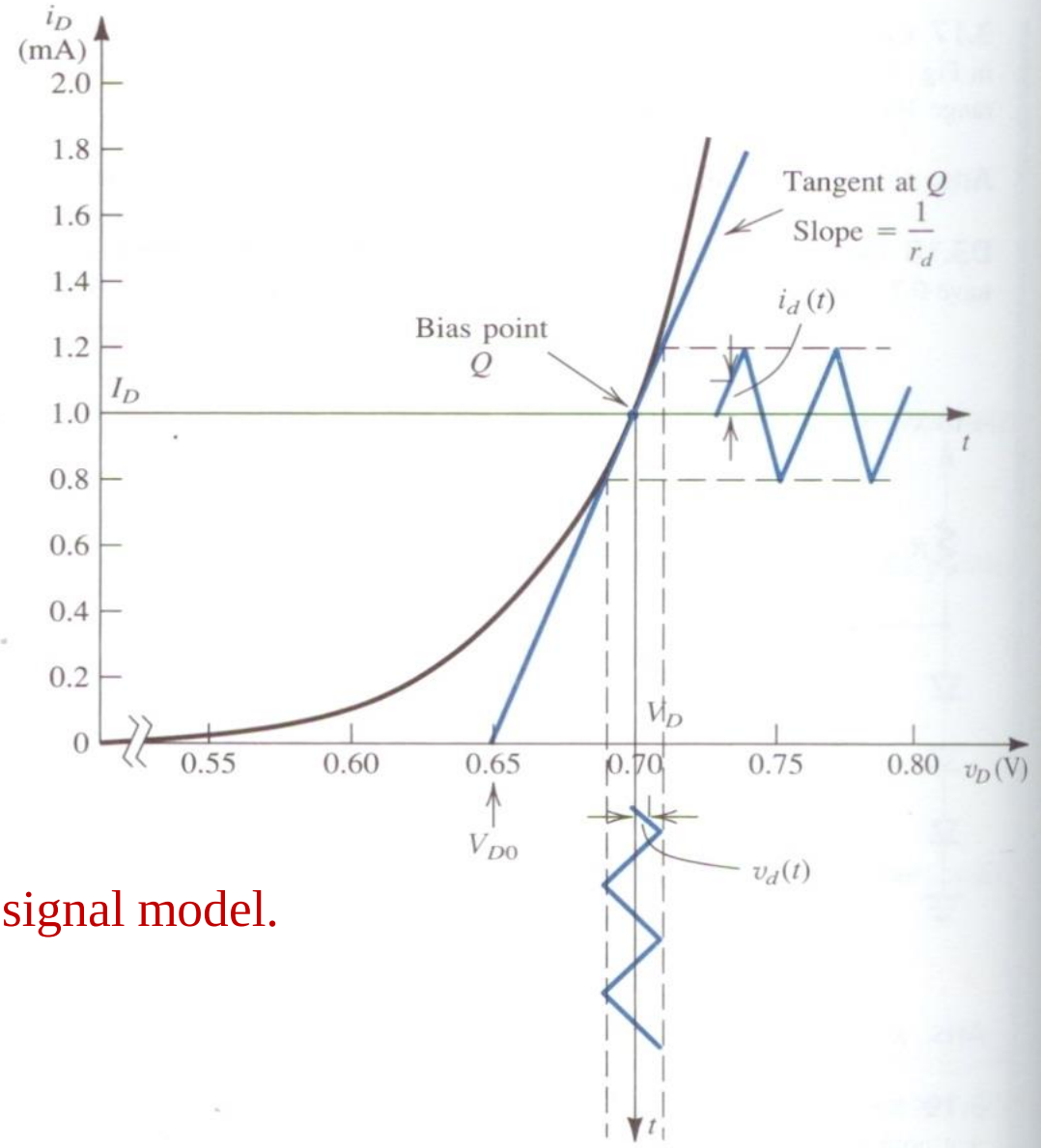
So the diode small-signal resistance is

$$r_d = \frac{nV_T}{I_D} = 1 / \left[\frac{\partial i_D}{\partial v_D} \right]_{i_D = I_D}$$

Since the signal excursion is restricted to a short, almost-linear segment of *I-V* characteristic around the bias point, the small signal model is **linear**.



(a)



Development of the diode small signal model.

The small signal approximation allows us to separate the dc analysis from the ac signal analysis.

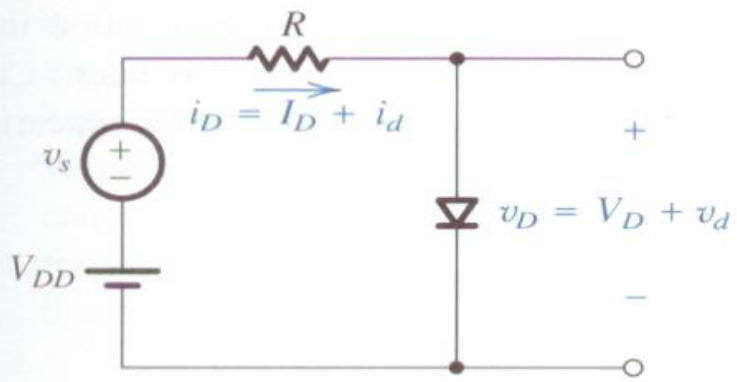
DC analysis: $V_{DD} = I_D R + V_D = I_D R + V_{D0} + I_D r_d$

V_{D0} is the dc point of the diode.

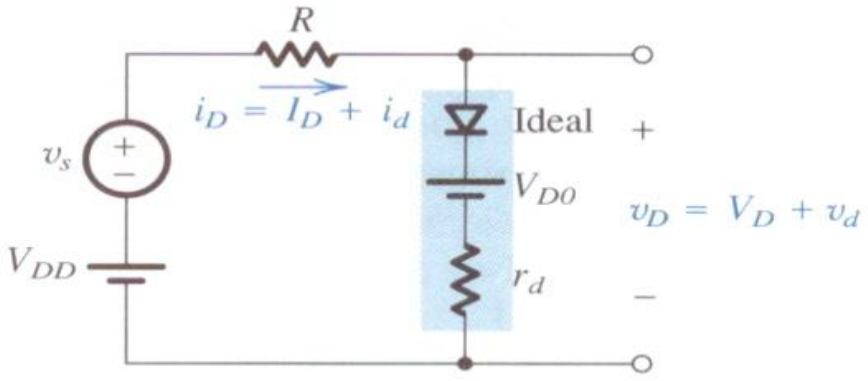
AC analysis: $v_s = i_d R + i_d r_d$

The signal analysis is performed by eliminating all dc sources and replacing the diode with its small signal resistance r_d.

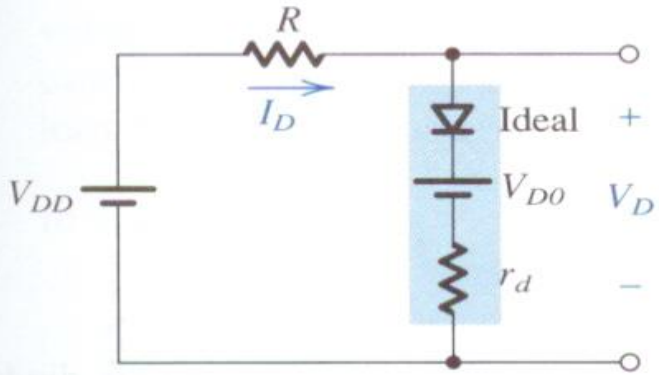
Small signal model is like piece-wise linear model.



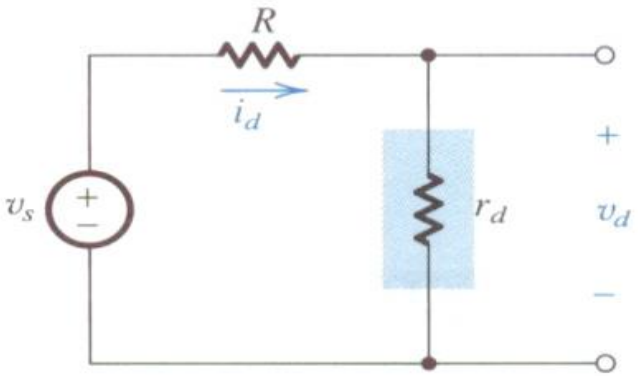
(a) Diode circuit



(b) Its equivalent model



(c) DC analysis



(d) AC analysis

Fig The analysis of the diode circuit.

Depletion capacitance

- We will see the analogy between depletion layer of a pn junction and a capacitor.
- As the voltage across the pn junction changes, the charge stored in the depletion layer changes accordingly.
- The depletion-layer charge can be derived by finding the charge stored on either side of the junction.

$$q_J = q_N = Q = qN_D x_n A$$

$$\frac{x_p}{x_n} = \frac{N_D}{N_A} \quad \Rightarrow \quad Q = q\frac{N_A N_D}{N_A + N_D} AW$$

$$x_n + x_p = W$$

$$W = \left\{ \frac{2\varepsilon_s (V_0 + V_R)}{e} \left[\frac{N_A + N_D}{N_A N_D} \right] \right\}^{1/2} \Rightarrow \quad C = \frac{dQ}{dV_R} = A\left\{ \frac{q\varepsilon_s N_A N_D}{2(V_0 + V_R)(N_A + N_D)} \right\}^{1/2}$$

With bias voltage across the diode,

$$W = \sqrt{\frac{2\varepsilon_{si}}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_0 - V_D)} \qquad V_D = -V_R$$

We can treat the depletion layer as parallel-plate capacitor and the junction capacitance is

$$C_j = \frac{\varepsilon_{si} A}{W} = \frac{C_{j0}}{\sqrt{1-\frac{V_D}{V_0}}}$$

$$C_{j0} = A\sqrt{\left(\frac{\varepsilon_{si} q}{2}\right)\left(\frac{N_A N_D}{N_A + N_D}\right)\left(\frac{1}{V_0}\right)}$$

C_{j0} is **the zero-voltage junction capacitance**.

More general form of the depletion capacitance is

$$C_j == \frac{C_{j0}}{\left(1-\frac{V_D}{V_0}\right)^m}$$

m is a constant whose value depends on the manner in which the concentration changes from the p to the n side of the junction. It is called **the grading coefficient**, and the value is from 1/3 to 1/2.

Under forward bias assume $V_D = \frac{V_0}{2}$

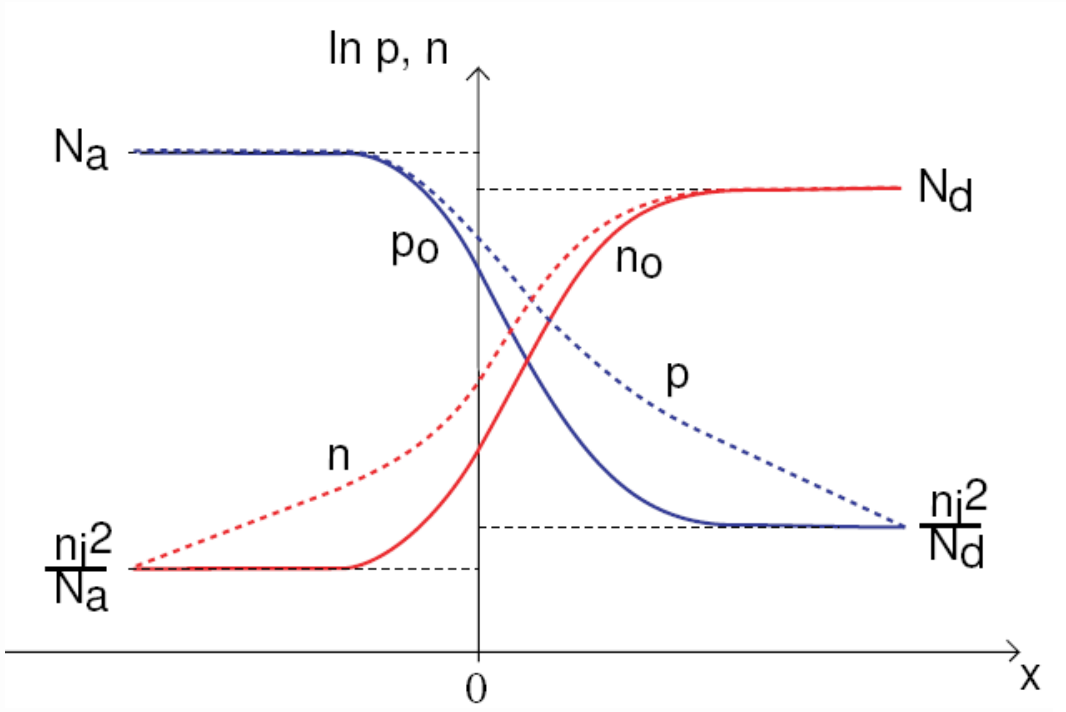
Junction capacitance is approximated by rules of thumb

$$C_j \cong \sqrt{2}C_{j0}$$

Diffusion capacitance

The excess minority-carrier charge is stored in both p and n bulk regions and depends on the terminal voltage.

Carrier picture for the forward bias:

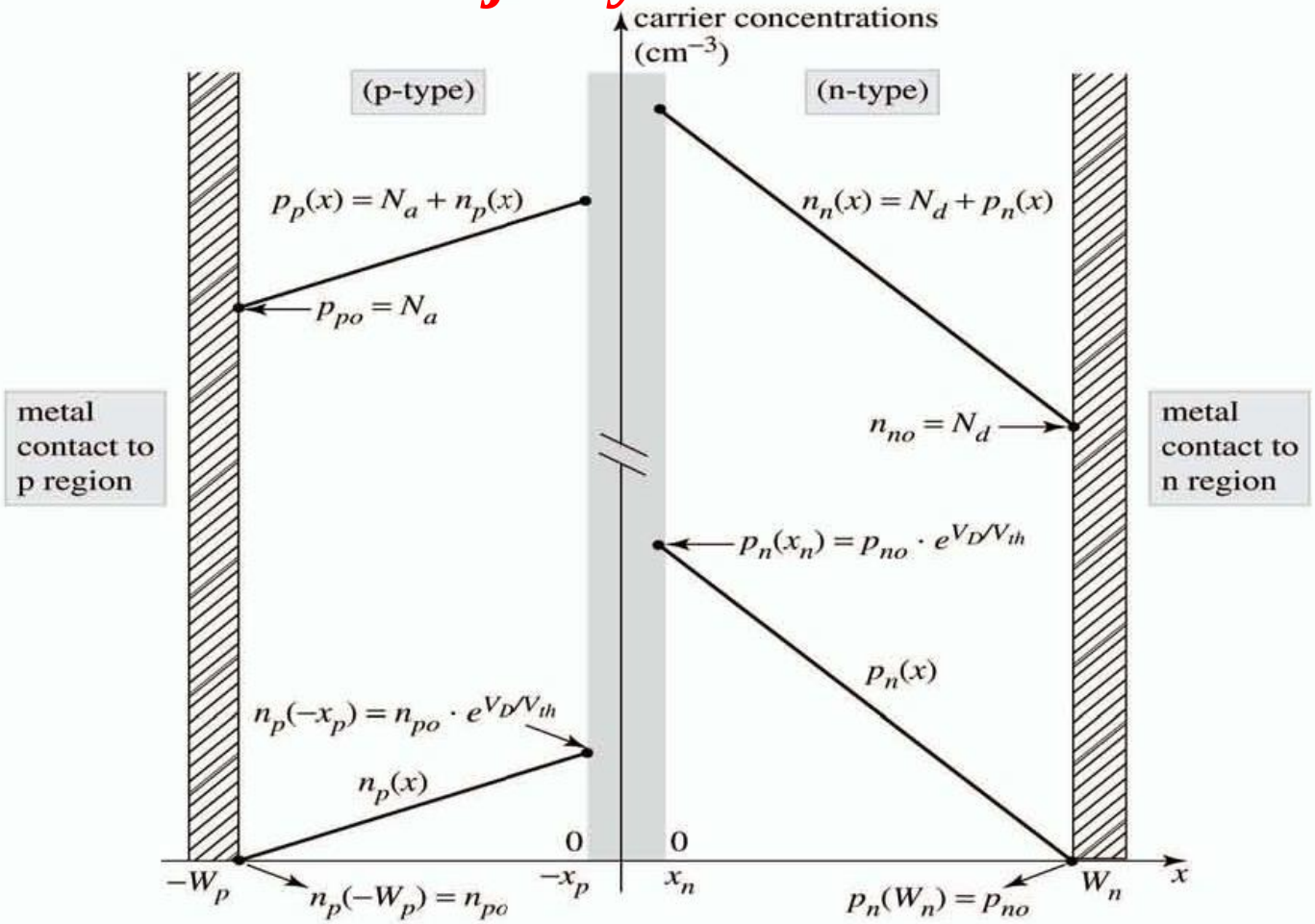


If QNR minority carrier concentration ↑ but majority carrier concentration **unchanged? ⇒ quasineutrality is violated.**

Quasineutrality demands that at every point in QNR:

Excess minority carrier concentration

=excess majority carrier concentration



In n-type Si, at every *x*:

$$p_n(x) - p_{n0} = n_n(x) - n_{n0}$$

In p-type Si, at every *x*:

$$n_p(x) - n_{p0} = p_p(x) - p_{p0}$$

Mathematically:

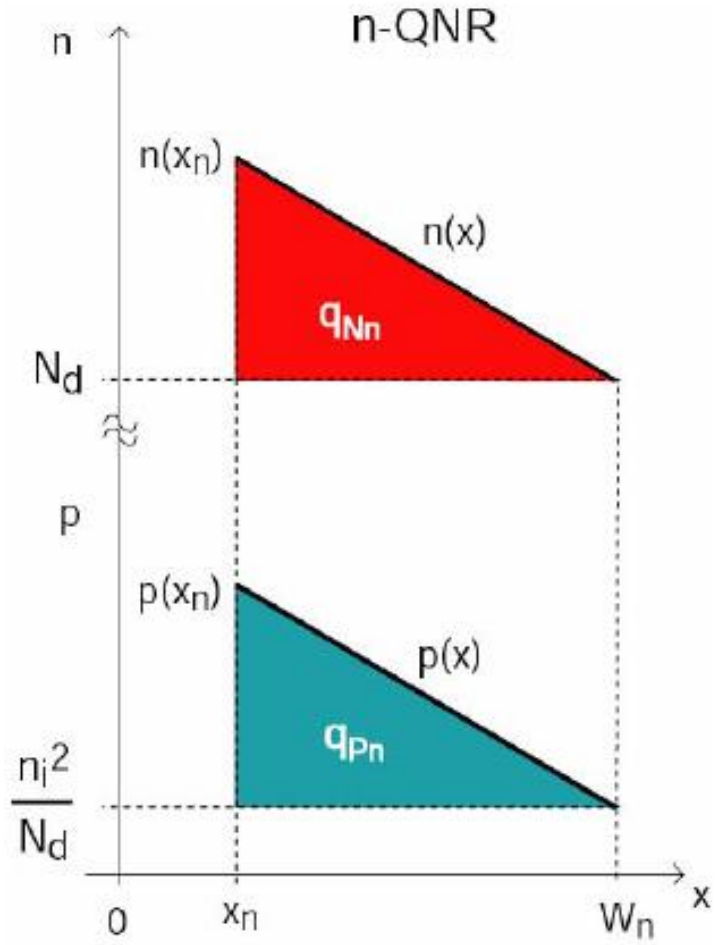
$$p_n'(x) = p_n(x) - p_{n0} \approx n_n'(x) = n_n(x) - n_{n0}$$

Define integrated carrier charge:

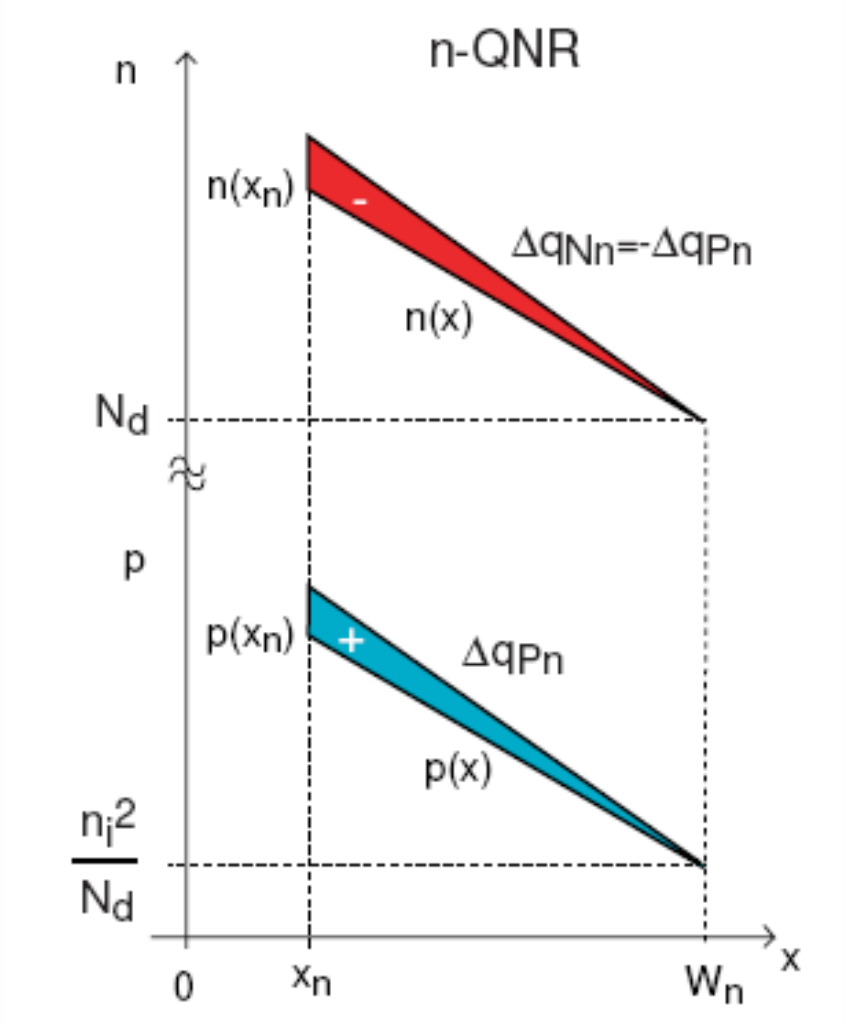
$$q_{Pn} = qA\frac{1}{2}P'(x_n)(W_n - x_n)$$

$$= \frac{1}{2}qA(W_n - x_n)(p(x_n) - p(W_n))$$

$$= \frac{1}{2}qA(W_n - x_n)p_{n0}(e^{V_D/V_{th}} - 1)$$



Now examine small increase in V_D:



Small increase in V_D
$\Rightarrow$ small increase in q_{Pn}
$\Rightarrow$ small increase in $|q_{Nn}|$

Behaves as capacitor of capacitance:

$$C_{dn} = \left.\frac{dq_{p_n}}{dv_D}\right|_{v_D=V_D}$$

$$= qA\frac{W_n - x_n}{2}\frac{n_i^2}{N_d}\frac{q}{kT}\exp[\frac{qV_D}{kT}]$$

The total diffusion capacitance C_d is the sum of the diffusion capacitance in n-QNR and p-QNR:

$$C_d = \left.\frac{-dq_{n_p}}{dv_D}\right|_{v_D} + \left.\frac{dq_{p_n}}{dv_D}\right|_{v_D}$$

$$= \frac{qA}{2V_{th}}\left[(W_p - x_p)n_{p0} + (W_n - x_n)p_{n0}\right]e^{v_D/V_{th}}$$

◆Under forward bias, the diffusion capacitance increases exponentially with the forward bias voltage.

◆Under reverse bias, the diffusion capacitance is nearly zero. This agrees with the reverse-bias carrier distribution which represent a tiny charge storage that furthermore is not a function of the diode voltage.

Can write in terms of I_{Dp} (portion of diode current due to holes in n_{QNR}):

$$J_p = q\frac{n_i^2}{N_d}\frac{D_p}{(W_n - x_n)}\exp[\frac{qV_D}{kT} - 1]$$

$$C_{dn} = \frac{q}{kT}\frac{(W_n - x_n)^2}{2D_p}qA\frac{n_i^2}{N_d}\frac{D_p}{(W_n - x_n)}\exp[\frac{qV_D}{kT}]$$

$$\approx \frac{q}{kT}\frac{(W_n - x_n)^2}{2D_p}I_{Dp}$$

Define **transit time of holes through n_{QNR}:** $\tau_{Tp} = \frac{(W_n - x_n)^2}{2D_p}$

Transit time is the average time for a hole to diffuse through n_{QNR}

For n_{QNR} $$C_{dn} \approx \frac{q}{kT}\tau_{Tp} I_{Dp}$$

Similarly for p_{QNR}: $$C_{dp} \approx \frac{q}{kT}\tau_{Tn} I_{Dn}$$

where the **transit time of electrons through p_{QNR}:**

$$\tau_{Tn} = \frac{(W_p - x_p)^2}{2D_n}$$

Both capacitors sit in **parallel ⇒ total diffusion capacitance:**

$$C_d = C_{dn} + C_{dp} = \frac{q}{kT}(\tau_{Tn} I_{Dn} + \tau_{Tp} I_{Dp})$$

$$C_d = (\tau_T / V_T) I_D$$

The diode high-frequency model

This model includes two capacitance: the depletion-layer capacitance C_j and the diffusion capacitance C_d.

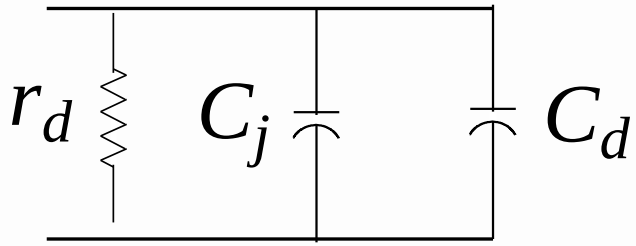


Fig. high-frequency small-signal model of the diode

Bias point: I_D, V_D

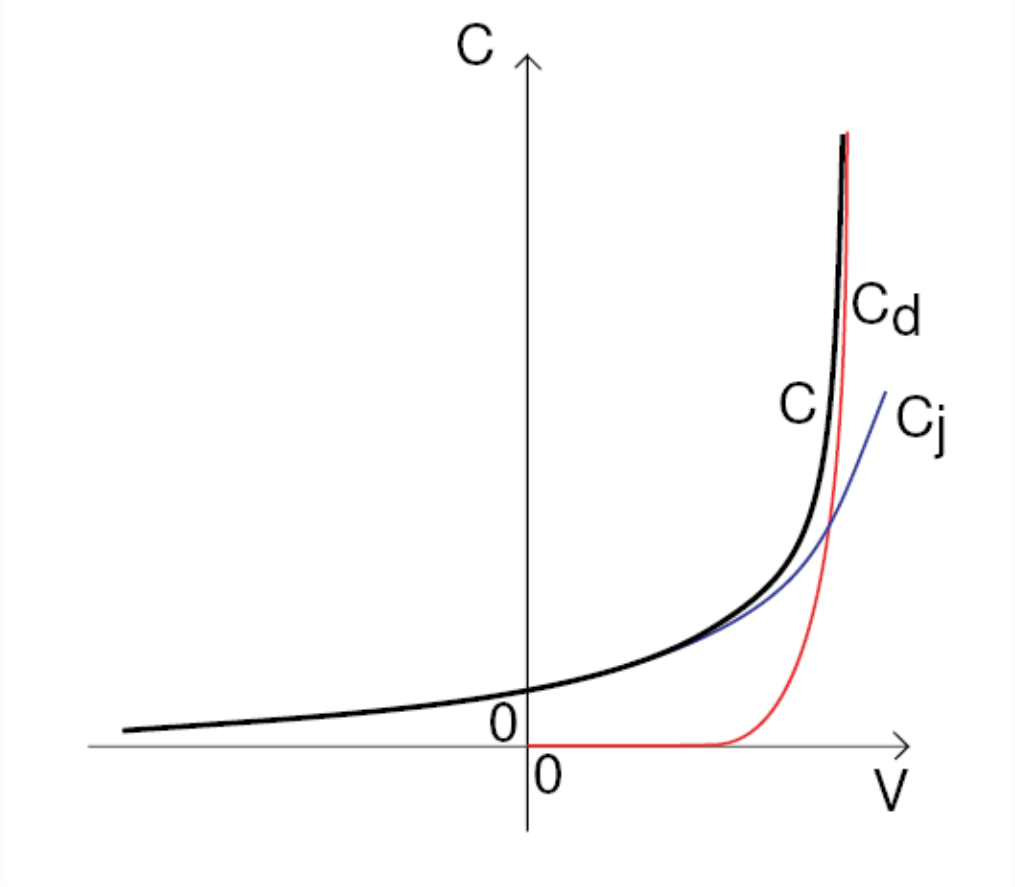
$$r_d = nV_T / I_D$$

$$C_d = (\tau_T / V_T) I_D$$

$$C_j = C_{j0} / (1 - \frac{V_D}{V_0})^m \text{ for } V_D < 0$$

$$C_j = 2C_{j0}, \text{ for } V_D > 0$$

Bias dependence of C_j and C_d:



- C_j dominates in reverse bias and small forward bias

$$\propto \frac{1}{\sqrt{\phi_B - V_D}}$$

- C_d dominates in strong forward bias

$$\propto e^{\left[\frac{qV_D}{kT}\right]}$$

Summary of small-signal model

- **Diode Current:** $I = I_0\left(e^{\left[\frac{qV_D}{kT}\right]} - 1\right)$
- **Conductance: associated with current voltage characteristics**
  - $g_d \propto I$ **in forward bias,**
  - g_d **negligible in reverse bias**
- **Junction capacitance: associated with charge modulation in depletion region**

$$C_j \propto \frac{1}{\sqrt{\phi_B - V_D}}$$

- **Diffusion capacitance: associated with charge storage in QNRs to maintain quasineutrality.**

$$C_d \propto e^{\left[\frac{qV_D}{kT}\right]}$$

Example

An IC diode is designed to have a room-temperature saturation current of $I_0=5\times10^{-17}A$ for a particular application. The fabrication process results in the device dimensions and physical parameters listed below.

Dimensions	Doping	Diffusion coefficient
$Wp=0.5\ um$	$Na=2.5X10^{17}cm^{-3}$	$Dn=14cm^2s^{-1}$
$Wn=1.0um$	$Nd=4.0X10^{16}cm^{-3}$	$Dp=10cm^2s^{-1}$

a) What diode area A is required for I_0?
b) Find the current and minority carrier concentrations at the edges of the depletion region for a forward bias $V_D=720\ mV$.
c) Plot the carrier concentration distribution along the diode.
d) Find the numerical values of the small-signal circuit elements for a bias voltage of $V_D=720mV$.

Solution:

(1) **Since the depletion width can be neglected**, the saturation current is

$$J_0 \cong qn_i^2\left(\frac{D_n}{N_aW_p}+\frac{D_p}{N_dW_n}\right)=5.79\times10^{-11}\ \text{A/cm}^2$$

Solving for the diode area from $I_0=J_0A$, we find that

$$A=8.64\times10^{-7}\ \text{cm}^2$$

(2) For a forward bias of $V_D=720\ mV$, the diode current is

$$I_D=I_0\left(e^{V_D/V_{th}}-1\right)=(5\times10^{-17}\,A)\cdot10^{720/60}=50\ \text{uA}$$

The minority carrier concentrations at the surfaces of QNRs are

$$p_{n0}=\frac{n_i^2}{N_d}=\frac{10^{20}}{4\times10^{16}}=2.5\times10^3\text{cm}^{-3}\qquad n_{p0}=\frac{n_i^2}{N_a}=\frac{10^{20}}{2.5\times10^{17}}=4\times10^2\text{cm}^{-3}$$

The minority carrier concentrations at the depletion region edges are

$$p_n(x_n)=p_{n0}10^{\log e(V_D/V_{th})}=2.5\times10^3\cdot10^{720/60}=2.5\times10^{15}\text{cm}^{-3}$$

$$n_p(-x_p)=n_{p0}10^{\log e(V_D/V_{th})}=4\times10^2\cdot10^{720/60}=4\times10^{14}\text{cm}^{-3}$$

(3) The majority carrier concentrations at the depletion region edges are

$$p_p(-x_p) = N_a + n_p(-x_p) = 2.5\times10^{17} + 4\times10^{14} = 2.504\times10^{17}\,\text{cm}^{-3}$$

$$n_n(x_n) = N_d + p_n(x_n) = 4\times10^{16} + 2.5\times10^{15} = 4.25\times10^{16}\,\text{cm}^{-3}$$

(4) The small-signal resistance

$$r_d = \frac{V_{th}}{I_D} = \frac{25mV}{50uA} = 500\Omega$$

The junction capacitance is

$$C_j = \frac{A\sqrt{\left(\frac{\varepsilon_{si}q}{2}\right)\left(\frac{N_A N_D}{N_A + N_D}\right)\left(\frac{1}{V_0}\right)}}{\left(1-\frac{V_D}{V_0}\right)^m} = 156\ \text{fF}$$

The diffusion capacitance is

$$C_d = \frac{qA}{2V_{th}}\left[(W_p - x_p)n_{p0} + (W_n - x_n)p_{n0}\right]e^{v_D/V_{th}} = 1.62\ \text{pF}$$

Homework 13

A one-sided p^+n silicon diode has doping concentrations of $N_a = 4 \times 10^{17}\ \text{cm}^{-3}$ and $N_d = 8 \times 10^{15}\ \text{cm}^{-3}$. The diode cross-sectional area is $A = 5 \times 10^{-4}\ \text{cm}^2$. (*a*) The maximum diffusion capacitance is to be limited to 1 nF. Determine (*i*) the maximum current through the diode, (*ii*) the maximum forward-bias voltage, and (*iii*) the diffusion resistance. (*b*) Repeat part (*a*) if the maximum diffusion capacitance is limited to 0.25 nF.

$$\tau_{n0} = 10^{-7}\,s \quad \tau_{p0} = 10^{-8}\,s \quad D_p = 10\text{cm}^2/s \quad D_n = 25\text{cm}^2/s$$

Assume the width of QNR regions are much larger than the width of the depletion region.

5. The application of diodes

- Voltage regulator
- Rectifier
- Limiting and clamping circuit

Use of the diode forward drop in voltage regulation (稳压器)

- What is voltage regulator?

  A voltage regulator is a circuit to provide a constant dc voltage between its output terminals in spite of

  (a) changes in the load current drawn from the regulator output terminal

  (b) changes in the dc power-supply voltage that feeds the regulator.

- Why can the diode be used in voltage regulator?

  The forward voltage drop of the diode remains almost constant at approximately 0.7V while the current through it varies relatively large amounts.

zener diodes

- Operation in the reverse breakdown region

- ✓ A diode can be designed as a voltage regulator due to the almost-constant voltage drop in the breakdown region.
- ✓ The diode operating in the breakdown region is called breakdown, more commonly, zener diodes.

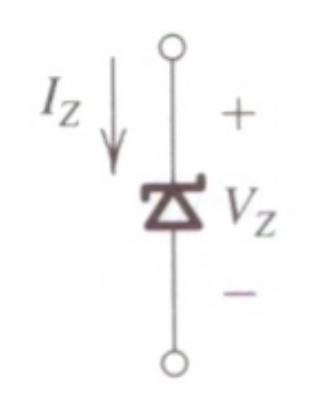


Fig Circuit symbol for a zener diode

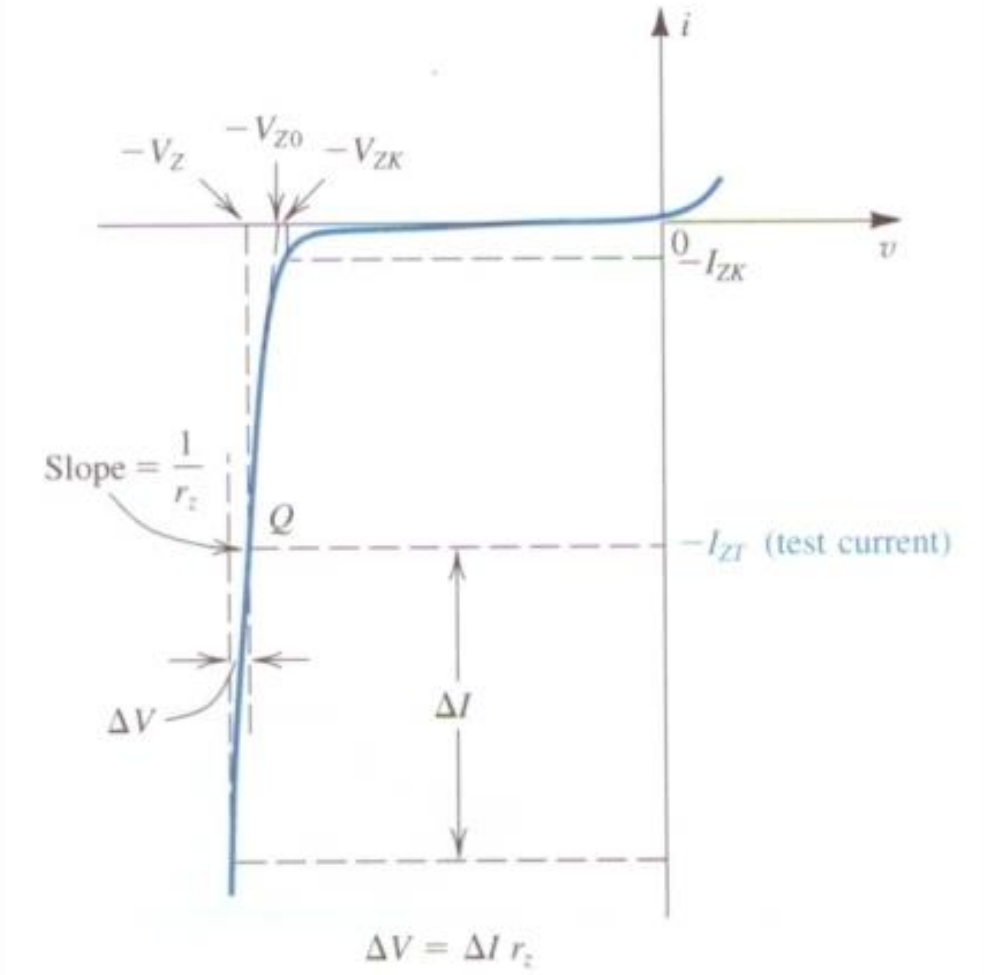


Fig The diode *I*-*V* characteristic with the breakdown region shown in some detail

The knee current I_{ZK} and the knee voltage V_{ZK}

$$V_Z = V_{Zk} + r_Z I_Z$$

rectifier circuits （整流电路）

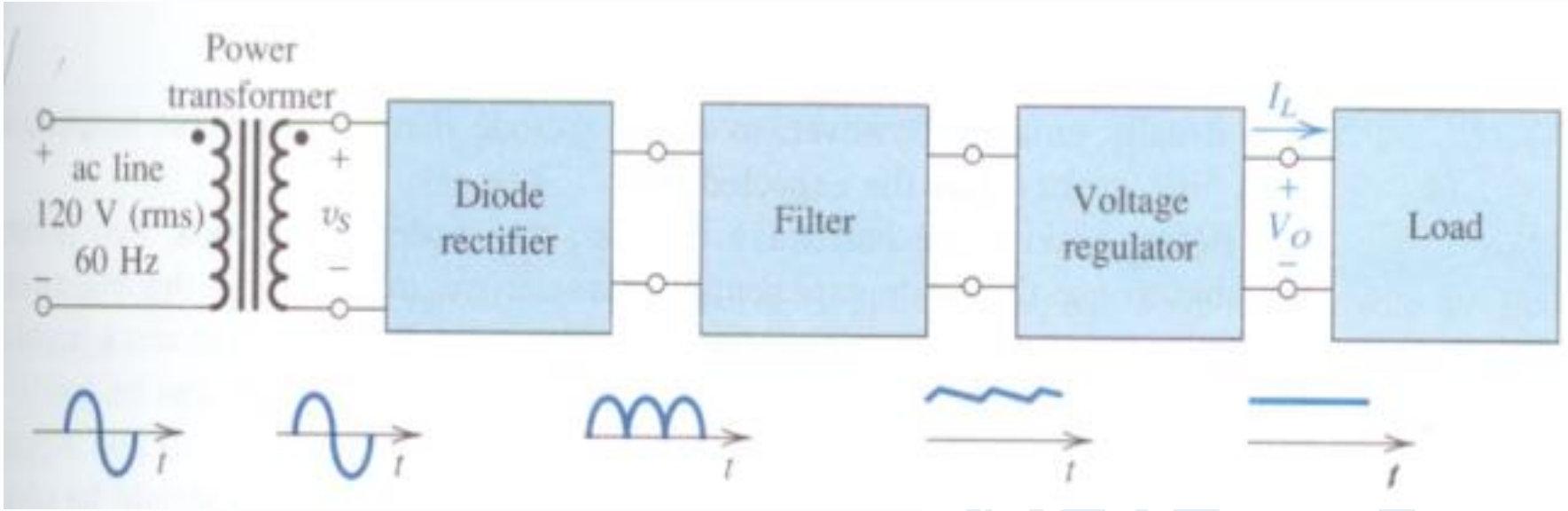


Fig Block diagram of a dc power supply

power transformer

- consists of two separated coils would around an iron core that magnetically couples the two windings.
- The primary winding has *N1* turns, and the second winding has *N2* turns.

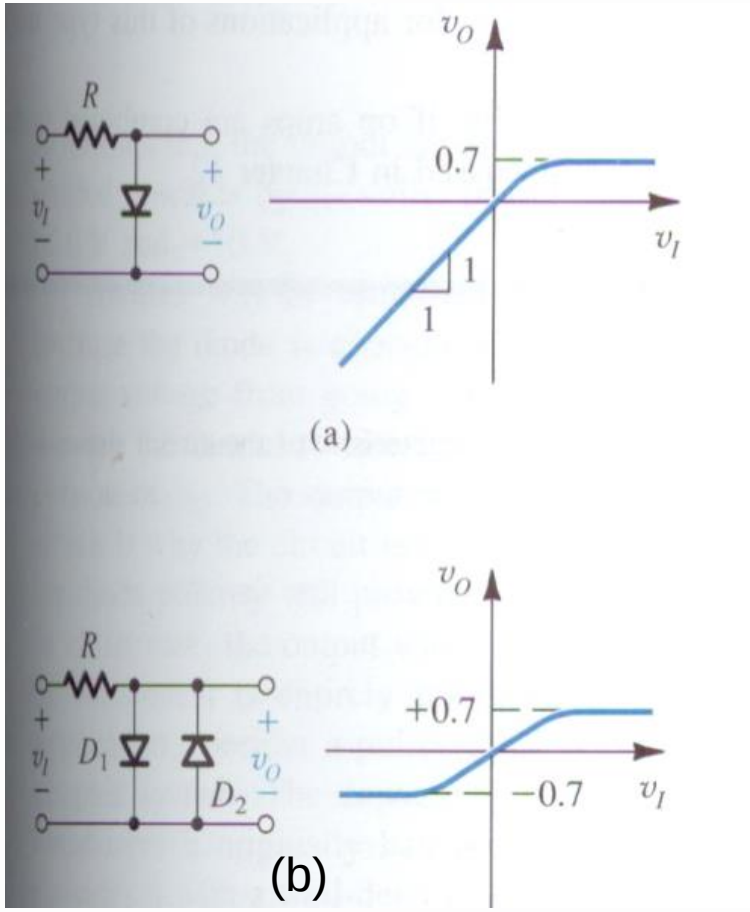
$$v_s = \frac{N2}{N1}120V$$

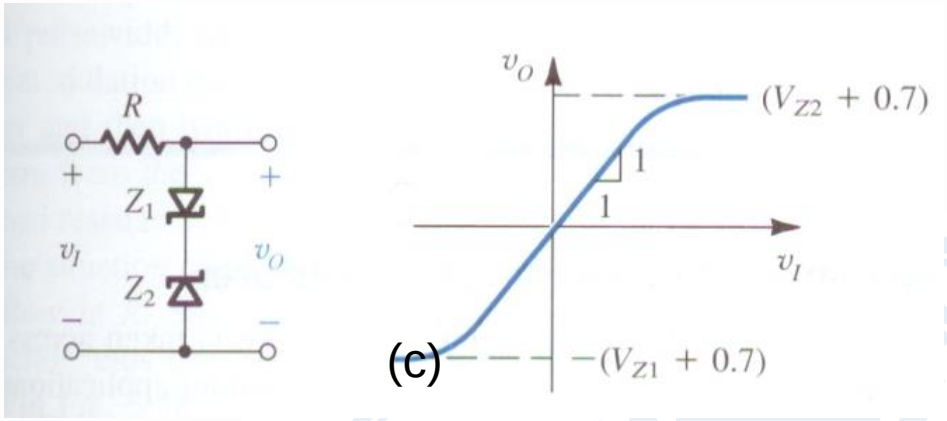
The diode rectifier converts the input sinusoid vs to a unipolar output, which has a dc component.

Filter is used to reduce the variation of the magnitude.

Finally **the voltage regulator** is employed to reduce ripple and stabilize the magnitude of the dc output voltage against variation caused by changes in load current.

Limiting and Clamping circuits
（钳位电路）





(a) half-wave rectifier
(b) double limiting
(c) double-anode zener

6. Special diodes types

- **The Schottky-barrier diode** (SBD) 肖特基势垒二极管

  It brings metal into contact with a moderately doped n-type semiconductor material. The resulting metal-semiconductor junction behaves like a diode.

  Two applications: 1) Gallium Arsenide (GaAs) circuits;

  2) bipolar-transistor logic circuits.

- **Varactors** (voltage-variable capacitors)

  Reverse-biased pn junctions exhibit a charge-storage effect that is modeled with the depletion-layer or junction capacitance C_j, which is a function of the reverse-biased voltage V_R.

- **Photodiodes**

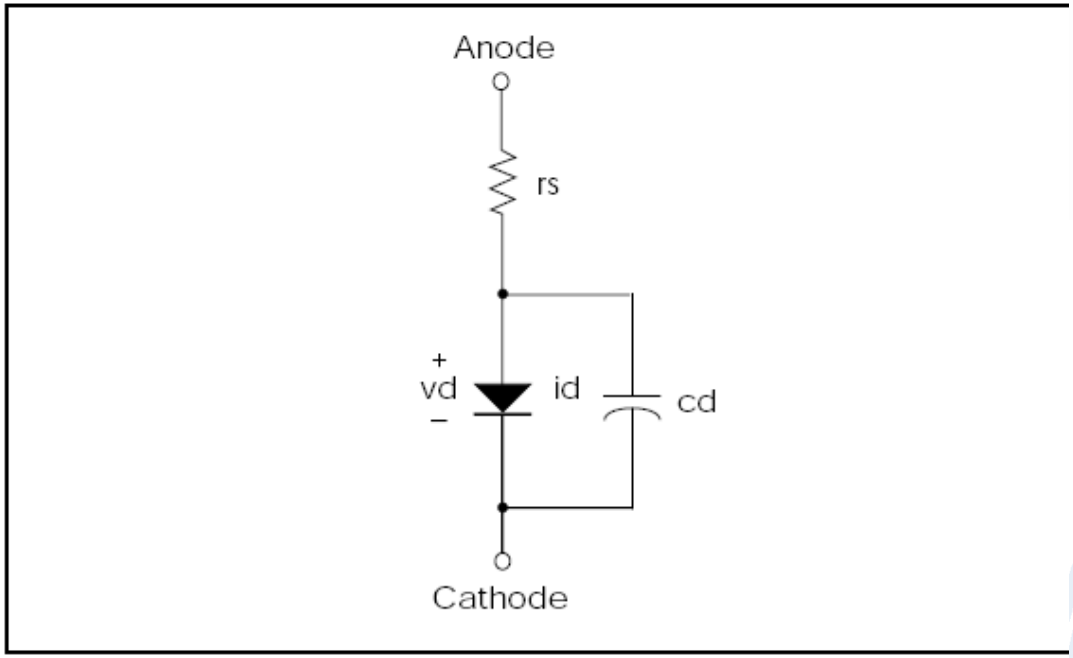
  A photodiode can be use to convert light signal into electrical signals.

  It is an important component of optoelectronics or photonics.

- **Light-Emitting Diodes** (LEDs)

  It converts a forward current into lights, as a inverse function of the photodiode.

7 . The SPICE diode model and simulation



$$id = ISeff \bullet (e^{\frac{vd}{N \bullet vt}} - 1)$$

The capacitance, *cd*, is a combination of diffusion capacitance, (*cdiff)*, depletion capacitance, *(cdep)*, metal, (*cmetal)*, and poly capacitances, *(cpoly)*.

$$cd = cdiff + cdep + cmetal + cpoly$$

.MODEL mname D <LEVEL = val> <keyword = val> ...

mname Model name. The diode element refers to the model by this name.
D Symbol that identifies a diode model
LEVEL Symbol that identifies a diode model
LEVEL=1 =junction diode
LEVEL=2 =Fowler-Nordheim
LEVEL=3 =geometric processing for junction diode

Table 3.3 SPICE DIODE MODEL PARAMETERS

Model Parameter	Symbol	SPICE Name	Units	Default Value
Saturation current	I_S	IS	A	1×10^{-14}
Emission coefficient	n	N	—	1
Ohmic resistance	R_S	RS	Ω	0
Built-in voltage	V_0	VJ	V	1
Zero-bias junction capacitance	C_{j0}	CJ0	F	0
Grading coefficient	m	M	—	0.5
Transit time	τ_T	TT	s	0
Breakdown voltage	V_{ZK}	BV	V	∞
Reverse current at V_{ZK}	I_{ZK}	IBV	A	1×10^{-10}

$$I_s = qAn_i^2\left(\frac{D_n}{N_a\left(W_p - x_p\right)} + \frac{D_p}{N_d\left(W_n - x_n\right)}\right)$$

$$\phi_B = \frac{kT}{q}\ln\left(\frac{N_a N_d}{n_i^2}\right)$$

$$C_{j0} = A\sqrt{\left(\frac{\varepsilon_{si} q}{2}\right)\left(\frac{N_A N_D}{N_A + N_D}\right)\left(\frac{1}{V_0}\right)}$$

$$\tau_{Tp} = \frac{(W_n - x_n)^2}{2D_p}$$

Table 14-2: Junction Diode Model Parameters (Level 1 and Level 3)

Function	Parameters
model type	LEVEL
DC parameters	IBV, IK, IKR, IS, ISW, N, RS, VB, RS
geometric junction	AREA, M, PJ
geometric capacitance (Level=3 only)	L, LM, LP, SHRINK, W, WM, WP, XM, XOJ, XOM, XP, XW
capacitance	CJ, CJP, FC, FCS, M, MJSW, PB, PHP, TT
noise	AK, KF

Setting Junction

Name (Alias)	Units	Default	Description

AREA		1.0	Junction area
			For LEVEL=1
			`AREAeff = AREA M, unitless`
			For LEVEL=3
			`AREAeff=AREA SCALM SHRINK M`
			`unit = meter`^{2}
			If you specify W and L:
			`AREAeff = Weff Leff M unit =`
			`meter`^{2}

EXPLI	amp/ AREAeff	1e15	Current explosion model parameter. The PN junction characteristics above the explosion current are linear, with the slope at the explosion point, which increases simulation speed and improves convergence. `EXPLIeff = EXPLI AREAeff`
IB	amp	1.0e-3	Current at breakdown voltage For LEVEL=3 `IBVeff = IBV AREAeff / SCALM`
IBV	amp	1.0e-3	Current at breakdown voltage For LEVEL=3 `IBVeff = IBV AREAeff / SCALM`
IK (IKF, JBF)	amp/ AREAeff	0.0	Forward knee current (intersection of the high- and low-current asymptotes) `IKeff = IK AREAeff.`
IKR (JBR)	amp/ AREAeff	0.0	Reverse knee current (intersection of the high- and low-current asymptotes) `IKReff = IKR AREAeff.`

Name (Alias)	Units	Default	Description
IS (JS)	amp/ AREAeff	1.0e-14	If you use an IS value less than EPSMIN, the program resets the value of IS to EPSMIN and displays a warning message. EPSMIN default=1.0e-28 If the value of IS is too large, the program displays a warning . For LEVEL=1 ISeff = AREAeff IS For LEVEL=3 ISeff = AREAeff IS/SCALM
JSW (ISP)	amp/ PJeff	0.0	Sidewall saturation current per unit junction periphery For LEVEL=1 JSWeff = PJeff JSW For LEVEL=3 JSWeff = PJeff JSW/SCALM
L			Default length of diode Leff = L SHRINK SCALM+ XWeff
LEVEL		1	Diode model selector LEVEL=1 or LEVEL=3 selects junction diode model LEVEL=2 selects Fowler-Nordheim model
N		1.0	Emission coefficient
PJ		0.0	Junction periphery For LEVEL=1 PJeff = PJ M, unitless For LEVEL=3 PJeff = PJ SCALM M SHRINK, meter If W and L are specified PJeff = (2 Weff + 2 Leff) M, meter

Name (Alias)	Units	Default	Description
RS	ohms or ohms/m^2 (see note below)	0.0	Ohmic series resistance For LEVEL=1 RSeff = RS/AREAeff For LEVEL=3 RSeff= RS·SCALM^2/AREAeff
SHRINK		1.0	Shrink factor
VB (BV, VAR, VRB)	V	0.0	Reverse breakdown voltage. 0.0 indicates an infinite breakdown voltage
XW			Accounts for masking and etching effects `XWeff = XW  SCALM`

Note: If you use a diode model for which the AREA is not specified, AREA defaults to 1; then RS has units of ohms. If AREA is specified in the netlist in m^2, then the units of RS are ohms/m^2.

Examples

.MODEL D1 D (CO=2PF, RS=1, IS=1P)
.MODEL DFOWLER D (LEVEL=2, TOX=100, JF=1E-10, EF=1E8)
.MODEL DGEO D (LEVEL=3, JS=1E-4, JSW=1E-8)
.MODEL d1n750a D
+ LEVEL=1 XP =0.0 EG =1.1
+ XOI =0.0 XOM =0.0 XM =0.0
+ WP =0.0 WM =0.0 LP =0.0
+ LM =0.0 AF =1.0 JSW =0.0
+ PB =0.65 PHP =0.8 M =0.2994
+ FC =0.95 FCS =0.4 MJSW=0.5
+ TT =2.446e-9 BV =4.65 RS =19
+ IS =1.485e-11 CJO =1.09e-9 CJP =0.0
+ PJ =0.0 N =1.615 IK =0.0
+ IKR =1.100e-2 IBV =2.00e-2

Example

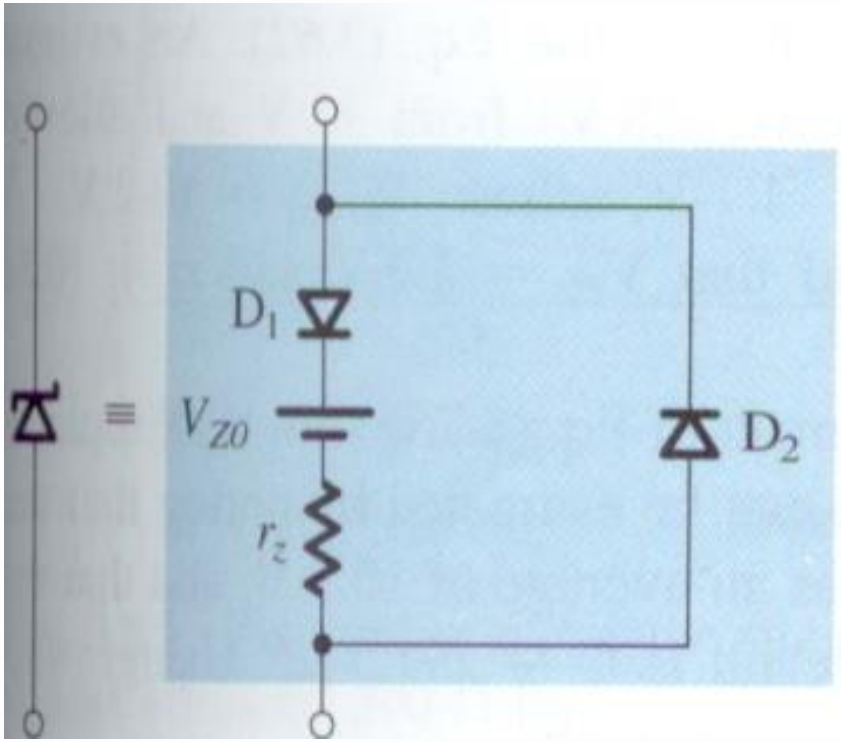
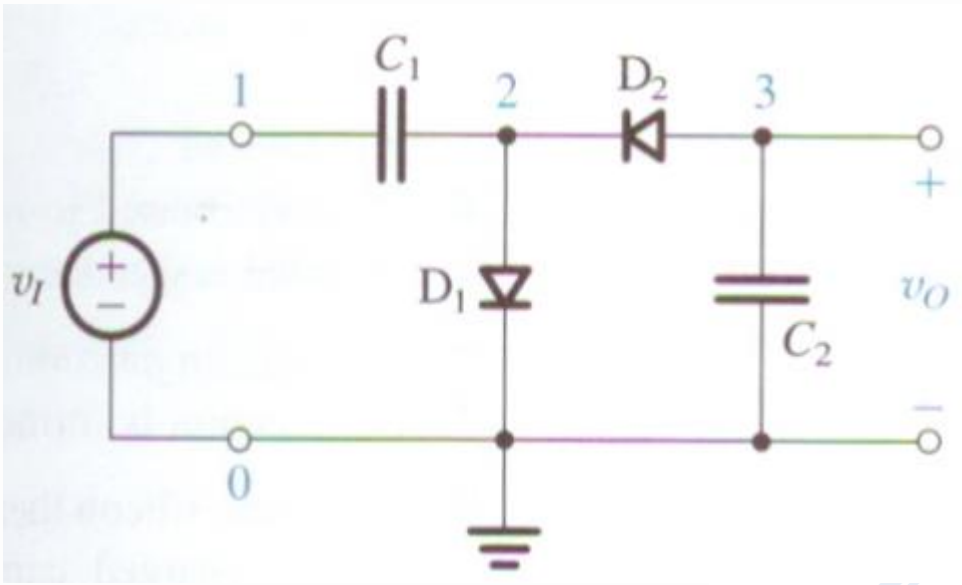


Fig Model for the zener diode. This model can be used in SPICE by defining the zener as a subcircuit. Diode *D*1 is ideal and can be approximated in SPICE by using n=0.01

```
* Zener diode_subcircuit
.subckt zener_diode 1          2
 *                        anode
  *                                cathode
Rz 3 4 10
Vz 2 3 4.9
D1 1 2 diode1
D2 1 4 diode_ideal
.model diode1 (IS=100pA n=1.679)
.model diode_ideal (IS=100pA n=0.01)
.ends zener_diode
```

Homework



The input is a sinusoid of *10* V peak and *1*KHz frequency.
The diodes are of the type (*IS=0.1pA*, *Rs=16ohm*, *Cjo=2 pF*, *Tt=12 ns*, *BV=100 V*, *IBV =0.1 pA*); the capacitors *C1=C2=1uF*.
Use SPICE to investigate the operation of the voltage doubler shown above. Plot the transient behavior of the voltages v_2 and v_o.