上海交通大学
SHANGHAI JIAO TONG UNIVERSITY

Lecture 13

MOS Electrostatics

Outline

- **Introduction to MOS structure**
- **Electrostatics of MOS in thermal equilibrium**
- **Electrostatics of MOS with applied bias**

Key questions

- What is the big deal about the metal-oxide-semiconductor structure?
- What do the electrostatics of the MOS structure look like at zero bias?
- How do the electrostatics of the MOS structure get modified if a voltage is applied across its terminals?

1. Introduction

Metal Oxide Semiconductor structure

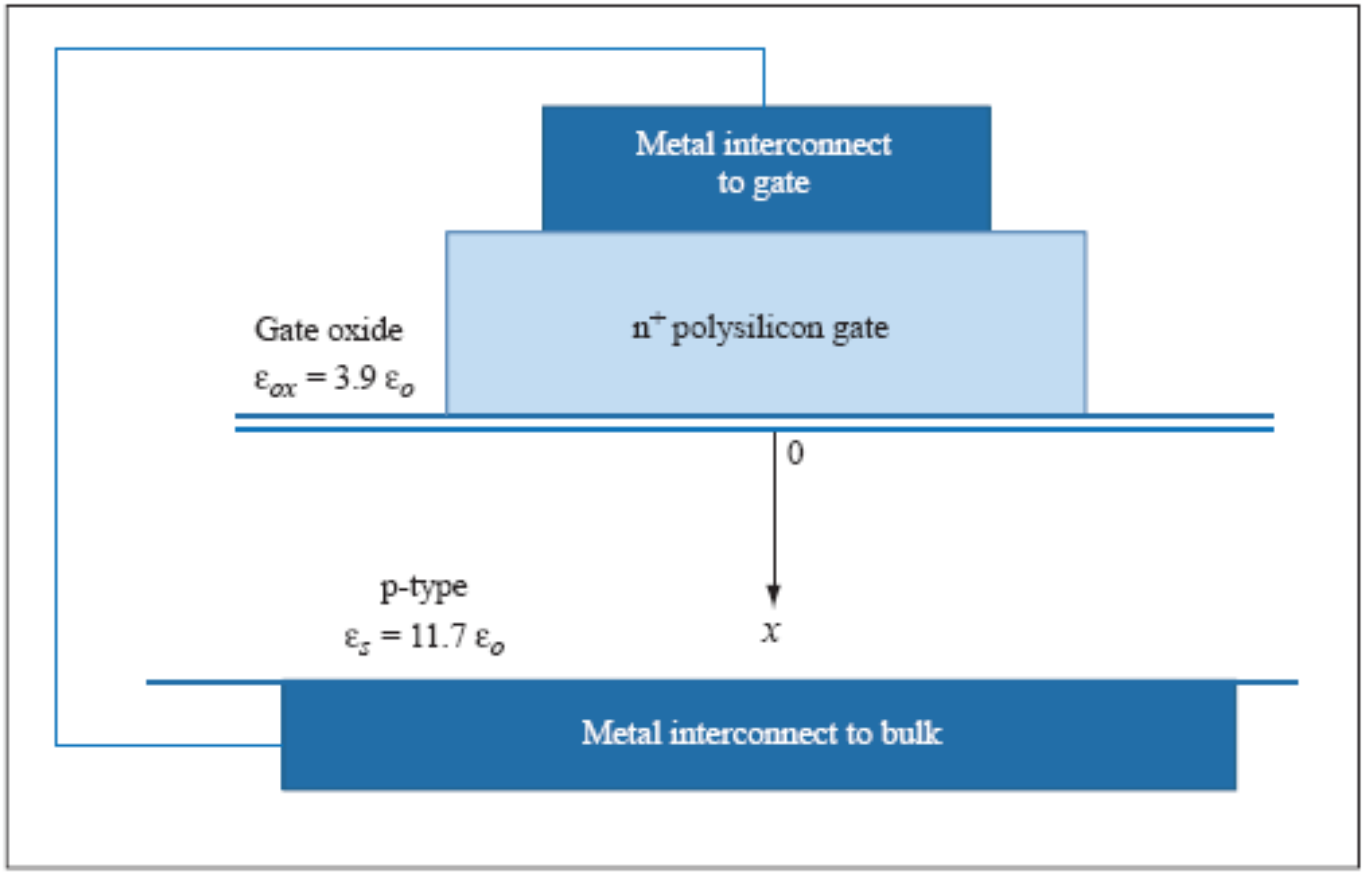


Fig by MIT OpenCoursesWare

MOS at the heart of the electronics revolution:

- **Digital and analog functions**

– Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is key element of Complementary Metal Oxide Semiconductor (CMOS) circuit family

- **Memory function**

– Dynamic Random Access Memory (DRAM)
– Static Random Access Memory (SRAM)
– Non Volatile Random Access Memory (NVRAM)

- **Imaging**

– Charge Coupled Device (CCD) and CMOS cameras

- **Displays**

– Active Matrix Liquid Crystal Displays (AMLCD)

Why the gate is made of polysilicon instead of metal?

- In the early days of PMOS technology, a metal gate was used.
  - it is difficult to align the metal over the channel precisely.
  - An offset creates a non-functioning transistor (either a short or an open)
- Today
  - A polysilicon material deposited before the source and drain diffusions is introduced to serve as a gate.
  - Source and drain is easy to align gate.
  - Gate is heavily doped to keep its resistance low and supposed to behave like a metal.

Metal: does not tolerate volume charge

– ⇒ charge can only exist at its surface

Oxide: insulator and does not have volume charge

– ⇒ no free carriers, no dopants

Semiconductor: can have volume charge

– ⇒ Space charge region (SCR)

In thermal equilibrium we assume Gate contact is shorted to Bulk contact. (i. e, $V_{GB} = 0V$)

-- Thermal equilibrium can't be established through oxide; need wire to allow transfer of charge between metal and semiconductor.

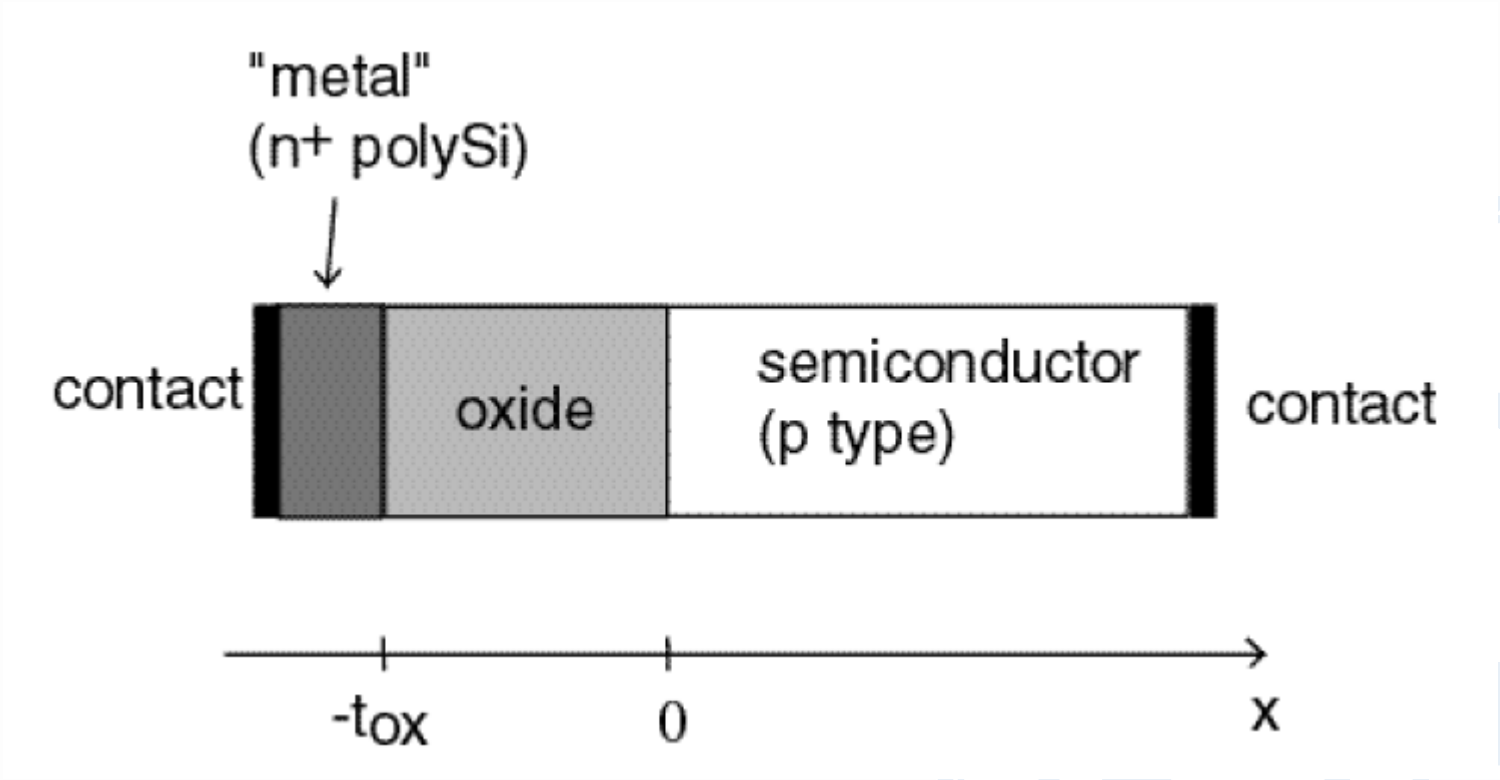
Technology development

- Horizontal device dimensions (channel length, source and drain area) are smaller and smaller
  - to maximize circuit density
  - To improve high-speed performance

- Vertical device dimensions are smaller and smaller
  - maintain field levels

2. MOS Electrostatics in equilibrium

Idealized 1D structure:



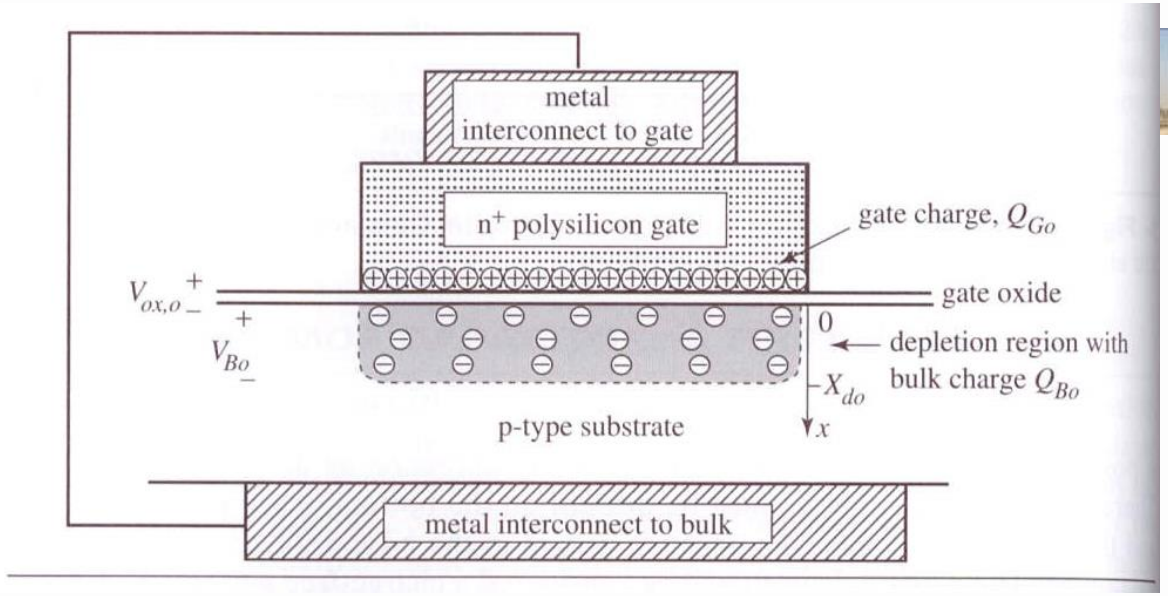


Fig Qualitative picture of charge distribution in an MOS capacitor with p-type substrate in thermal equilibrium

We interconnect gate to substrate to let $V_D=0$ (the applied voltage is zero), which is a necessary condition for equilibrium.

Since gate is heavily doped with donors, $\phi_{n+} = 550$ mV

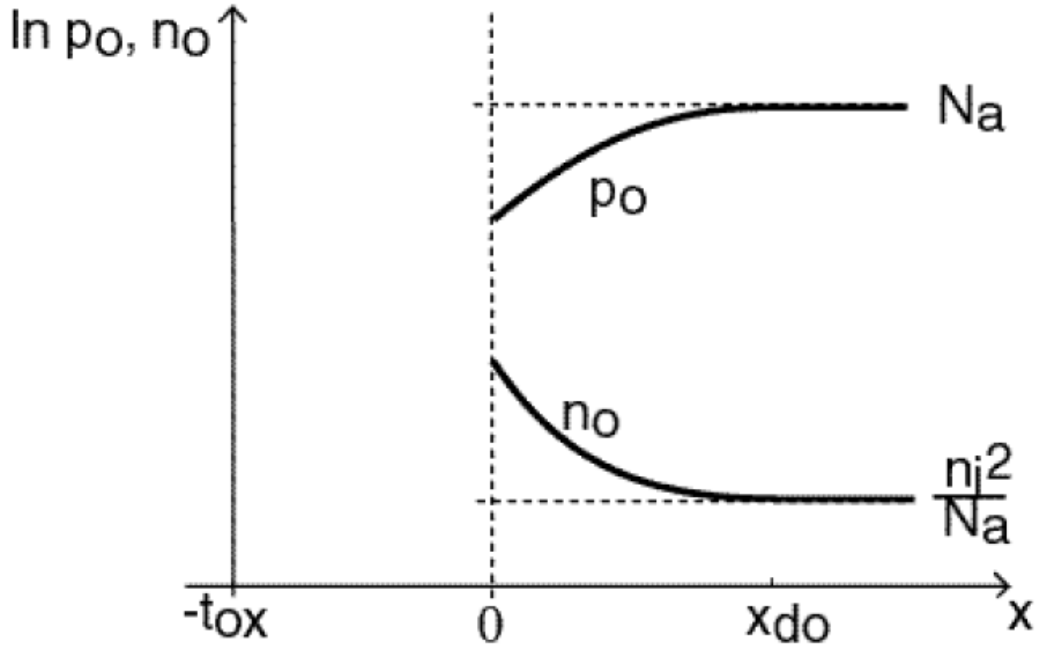
The potential of p-type substrate is $\phi_p = -V_{th} \ln\left(\frac{N_a}{n_i}\right)$

So the electric field E_0 is positive, resulting positive charges on the bottom of the gate and negative charges in the p-type silicon underlying the gate oxide to balance it.

An intuitive understanding of depletion region is the positive charges of the gate repel holes and leave the immobile negatively-charged acceptors.

For most metals on p-Si, equilibrium achieved by electrons flowing from metal to semiconductor and holes from semiconductor to metal:

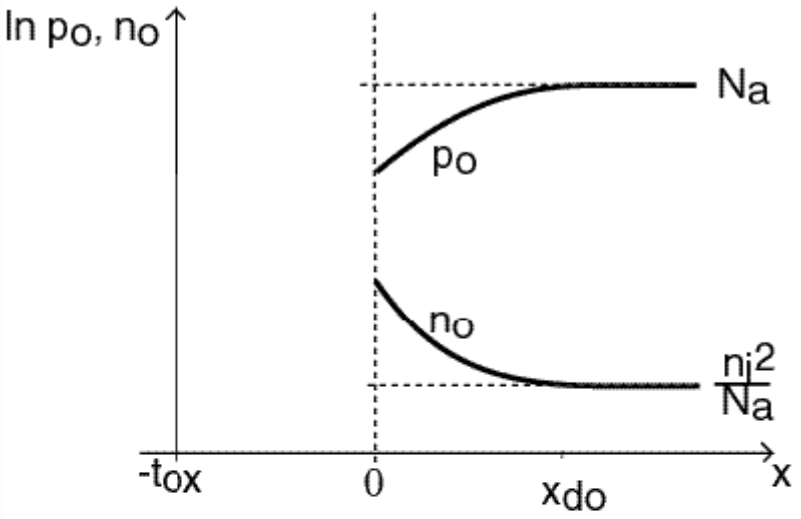
Remember : $n_0 p_0 = n_i^2$

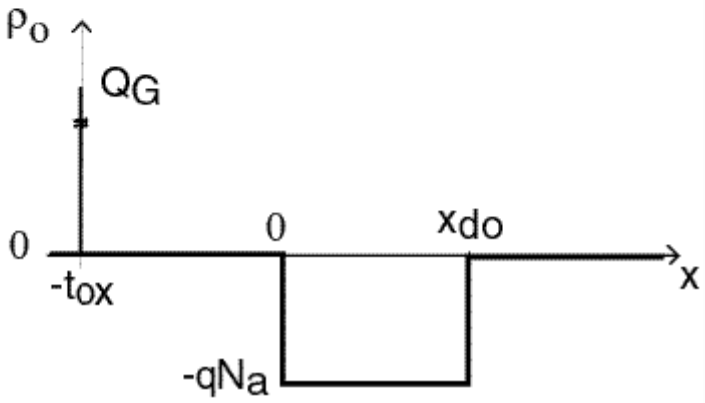


Fewer holes near Si/SiO_2 interface

⇨ **Ionized acceptors exposed (*volume charge*)**

Space Charge Density





- In semiconductor: space charge region close Si /SiO_2 interface – can use **depletion approximation**
- In metal: sheet of charge at metal /SiO_2 interface
- Overall charge neutrality

$$x = -t_{ox}; \qquad \sigma = Q_G$$

$$-t_{ox} < x < 0; \qquad \rho_0(x) = 0$$

$$0 < x < x_{do}; \qquad \rho_0(x) = -qN_a$$

$$x > x_{do}; \qquad \rho_0(x) = 0$$

Electric Field

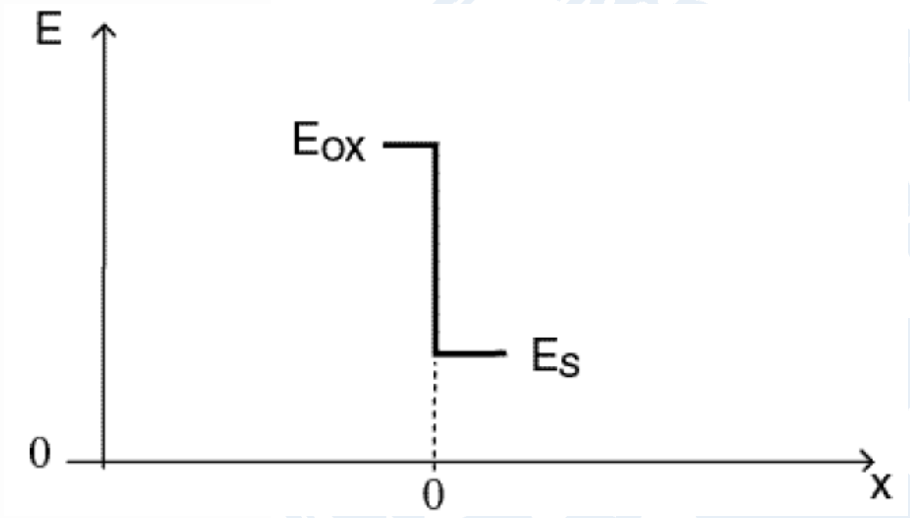
Integrate Poisson's equation

$$E_o(x_2) - E_o(x_1) = \frac{1}{\varepsilon}\int_{x_1}^{x_2} \rho(x')dx'$$

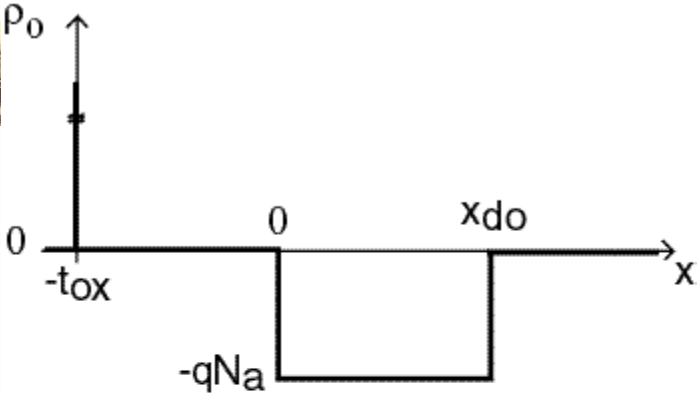
At interface between oxide and semiconductor, there is a change in **permittivity ⇒ change in electric field**

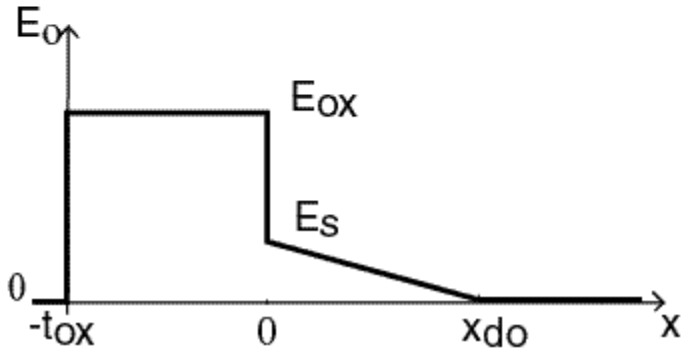
$$\varepsilon_{ox} E_{ox} = \varepsilon_s E_s$$

$$\frac{E_{ox}}{E_s} = \frac{\varepsilon_s}{\varepsilon_{ox}} \approx 3$$



Start integrating from deep inside semiconductor:





$x > x_{do};$ $\quad E_o(x) = 0$

$0 < x < x_{do};$ $\quad E_o(x) - E_o(x_{do}) = \frac{1}{\varepsilon_s}\int_{x_{do}}^{x} -qN_a dx' = -\frac{qN_a}{\varepsilon_s}(x - x_{do})$

$-t_{ox} < x < 0;$ $\quad E_o(x) = \frac{\varepsilon_s}{\varepsilon_{ox}} E_o(x = 0^+) = \frac{qN_a x_{do}}{\varepsilon_{ox}}$

$x < -t_{ox};$ $\quad E(x) = 0$

Electrostatic Potential

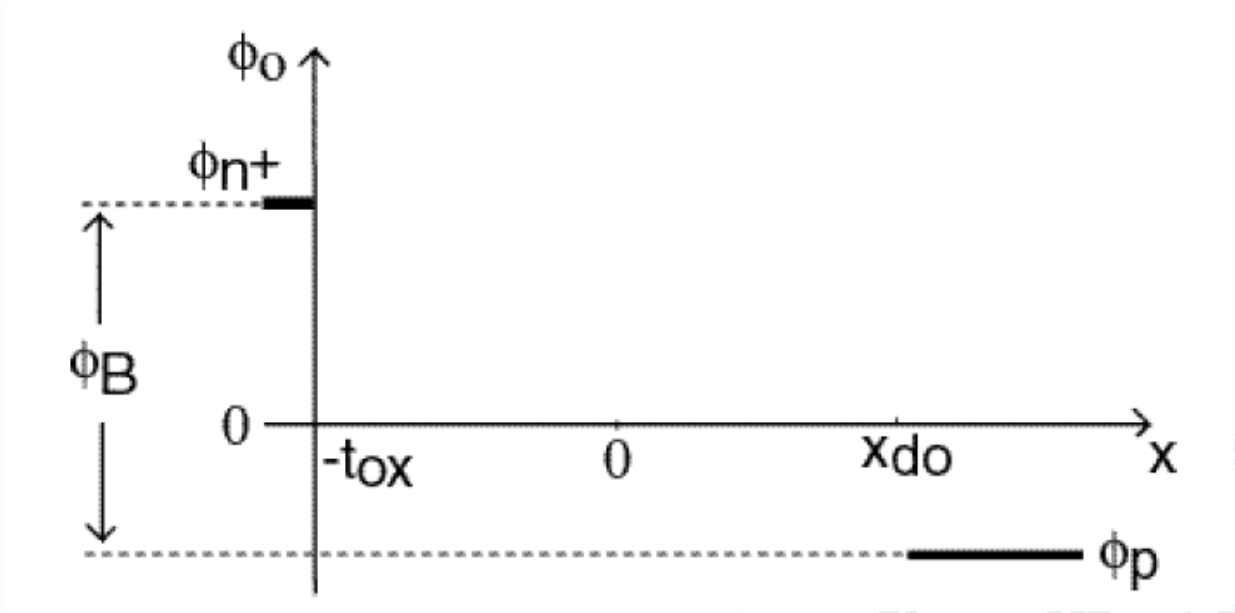
With $\phi = 0$ @n_o=p_o=n_i

$$\phi = \frac{kT}{q} \bullet \ln \frac{n_0}{n_i} \qquad \phi = -\frac{kT}{q} \bullet \ln \frac{p_0}{n_i}$$

In QNRs, n_o and p_o are known ⇒ can determine φ

$$\text{in p-QNR: } p_0 = N_a \Rightarrow \phi_p = -\frac{kT}{q} \bullet \ln \frac{N_a}{n_i}$$

$$\text{in n}^+\text{-gate: } n_0 = N_d^+ \Rightarrow \phi_g = \phi_{n^+}$$

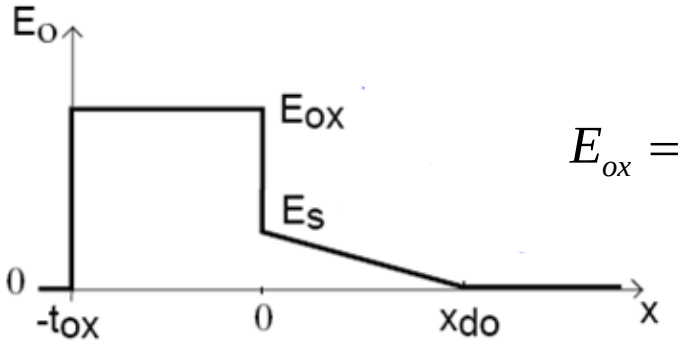


Built-in potential:

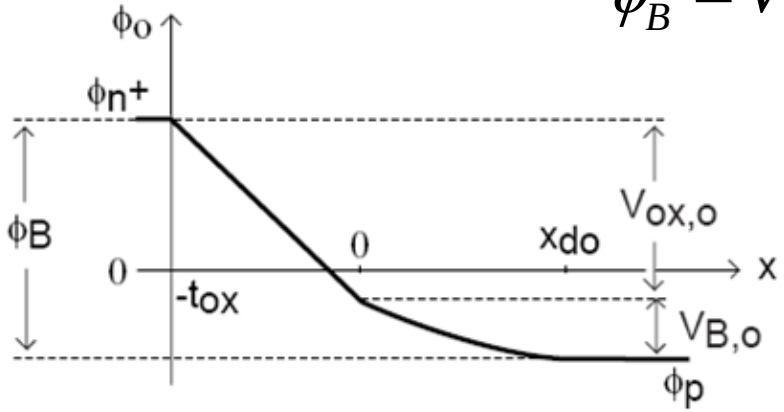
$$\phi_B = \phi_g - \phi_p = \phi_{n^+} + \frac{kT}{q} \bullet \ln \frac{N_a}{n_i}$$

To obtain $\varphi_o(x)$, integrate $E_o(x)$; start from deep inside semiconductor bulk:

$$\phi_o(x_2)-\phi_o(x_1)=-\int_{x_1}^{x_2} E_o(x')dx'$$



$$E_{ox}=\frac{qN_a x_{do}}{\varepsilon_{ox}} \qquad E_s=\frac{qN_a x_{do}}{\varepsilon_s}$$



$$\phi_B=V_{B,o}+V_{ox,o}=\frac{qN_a x_{do}^2}{2\varepsilon_s}+\frac{qN_a x_{do} t_{ox}}{\varepsilon_{ox}}$$

$$x > x_{do;} \qquad \phi_o(x) = \phi_p$$

$$0 < x < x_{do}; \qquad \phi_o(x) - \phi_o(x_{do}) = -\int_{x_{do}}^{x} -\frac{qN_a}{\varepsilon_s}(x' - x_{do})dx'$$

Surface potential $\phi_s = \phi(0)$ $\phi_o(x) = \phi_p + \frac{qN_a}{2\varepsilon_s}(x' - x_{do})^2$

$$AT \quad x = 0 \qquad \phi_o(0) = \phi_p + \frac{qN_a}{2\varepsilon_s}(x_{do})^2$$

$$-t_{ox} < x < 0; \qquad \phi_o(x) = \phi_p + \frac{qN_a}{2\varepsilon_s}(x_{do})^2 + \frac{qN_a x_{do}}{\varepsilon_{ox}}(-x)$$

$$x < -t_{ox}; \qquad \phi_o(x) = \phi_n$$

Still do not know x_{do}⇒need one more equation

Potential difference across structure has to add up to φ_B:

$$\phi_B = V_{B,o} + V_{ox,o} = \frac{qN_a x_{do}^2}{2\varepsilon_s} + \frac{qN_a x_{do} t_{ox}}{\varepsilon_{ox}}$$

Solve quadratic equation:

$$x_{do} = \frac{\varepsilon_s}{\varepsilon_{ox}} t_{ox} \left[\sqrt{1 + \frac{2\varepsilon_{ox}^2 \phi_B}{q\varepsilon_s N_a t_{do}^2}} - 1 \right]$$

$$= \frac{\varepsilon_s}{C_{ox}} \left[\sqrt{1 + \frac{2C_{ox}^2 \phi_B}{q\varepsilon_s N_a}} - 1 \right]$$

where C_{ox} is the capacitance per unit area of oxide

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

rewrite

$$x_{do} = \frac{\varepsilon_s}{\varepsilon_{ox}} t_{ox} \left[\sqrt{1 + \frac{2\varepsilon_{ox}^2 \phi_B}{q\varepsilon_s N_a t_{do}^2}} - 1 \right] = \frac{\varepsilon_s}{C_{ox}} \left[\sqrt{1 + \frac{4\phi_B}{\gamma^2}} - 1 \right]$$

where γ is **body factor coefficient** units: $V^{+1/2}$

$$\gamma = \frac{1}{C_{ox}} \sqrt{2\varepsilon_s q N_a}$$

Numerical example:

$$N_d = 10^{20} cm^{-3}, N_a = 10^{17} cm^{-3}, t_{ox} = 8nm$$

$$\phi_B = 550mV + 420mV = 970mV$$

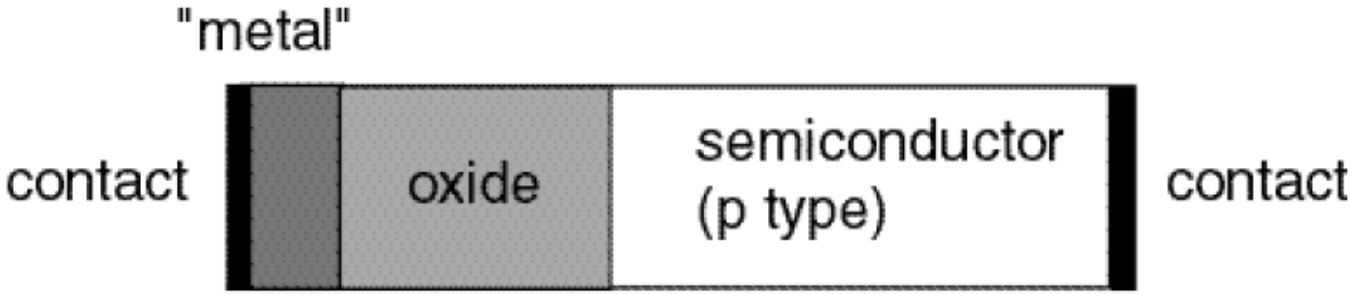
$$C_{ox} = 4.3 \times 10^{-7} F / cm^2$$

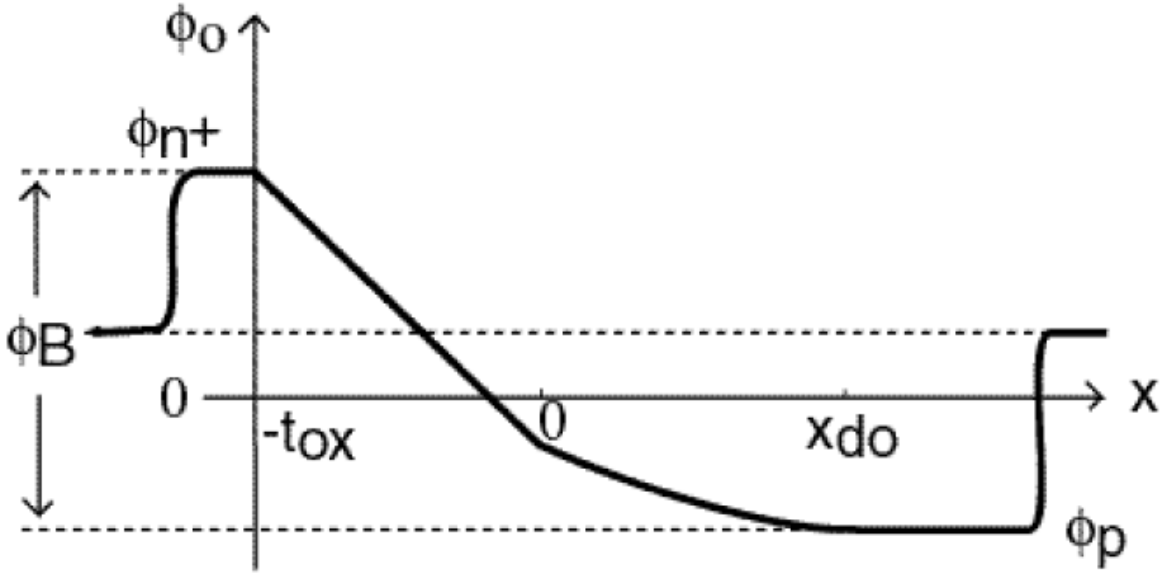
$$\gamma = 0.43V^{1/2}$$

$$x_{do} = 91nm$$

There are also contact potentials

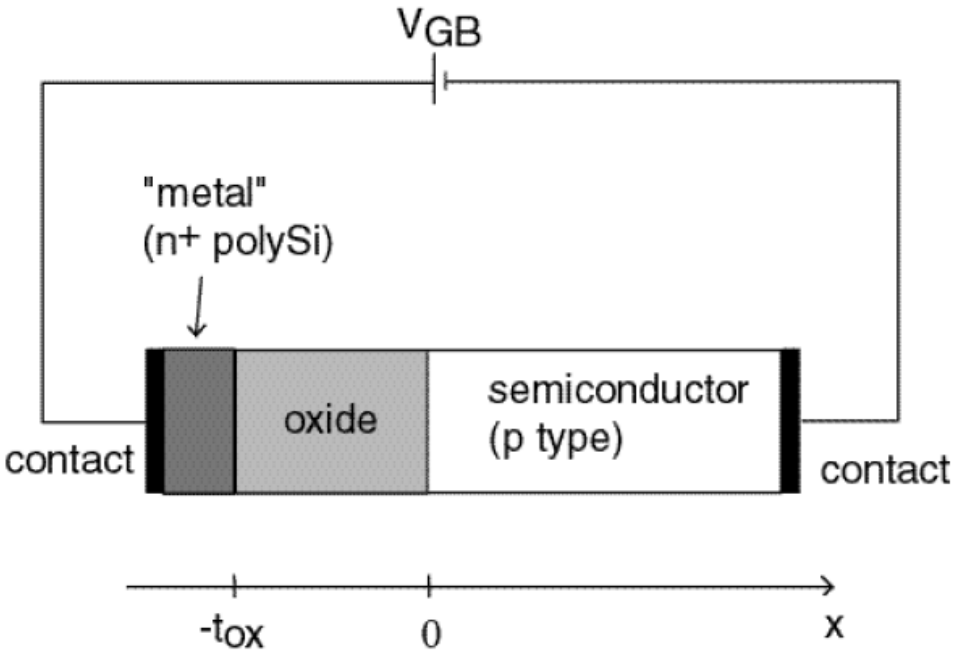
⇒ total potential difference from contact to contact is zero!





3. MOS with applied bias V_{GB}

Apply voltage to gate with respect to semiconductor:



Electrostatics of MOS structure affected

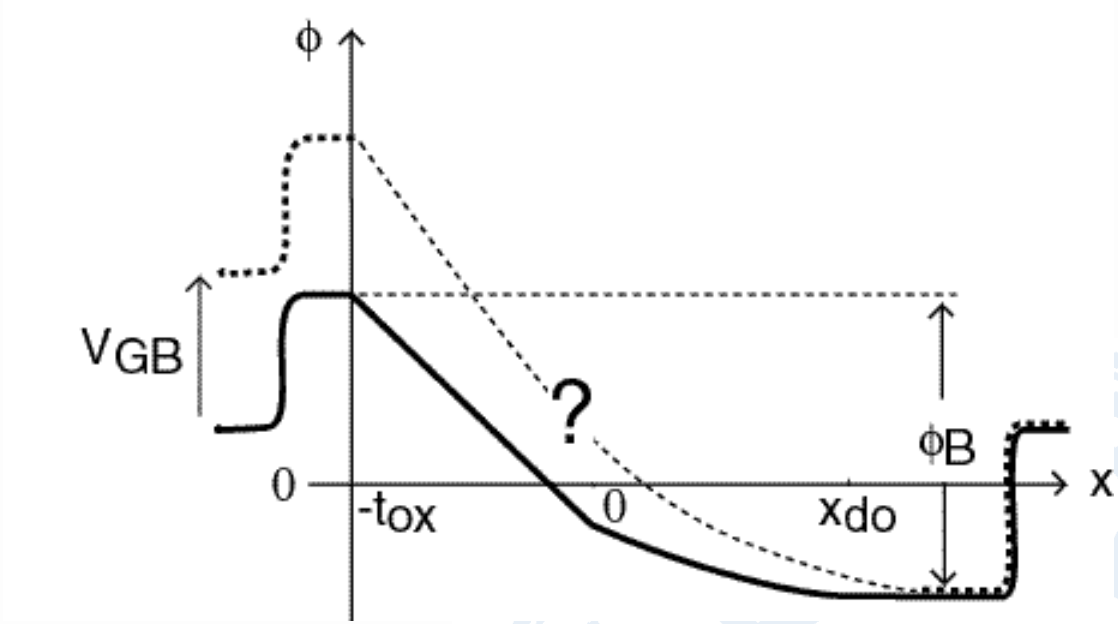
⇒ potential difference across entire structure now ≠ 0

How is potential difference accommodated?

Potential can drop in:

- gate contact
- n^+-polysilicon gate
- oxide
- semiconductor SCR
- semiconductor QNR
- semiconductor contact

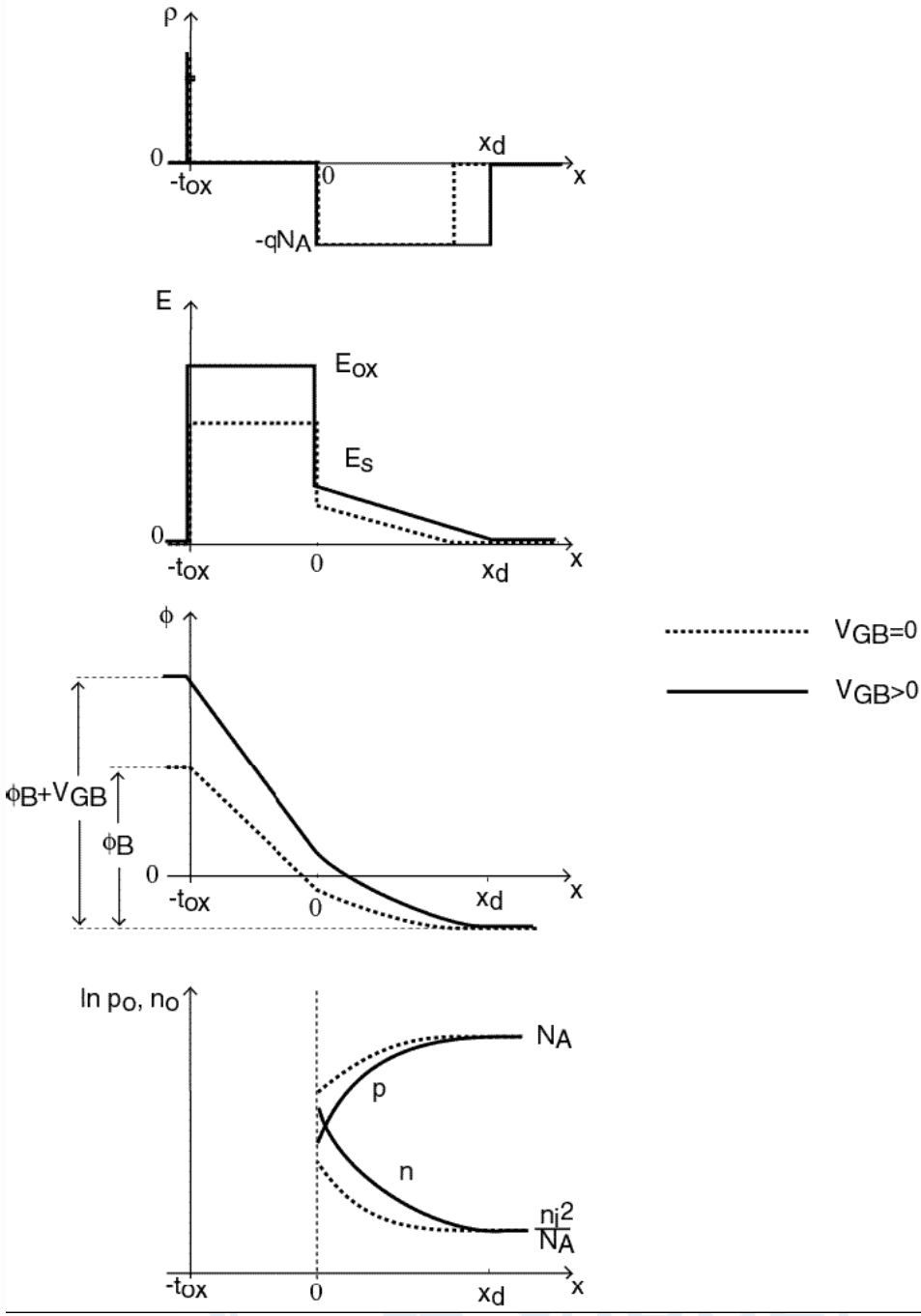
Potential difference shows up across oxide and SCR in semiconductor



- Oxide is an insulator
  ⇒ no current anywhere in structure
- In SCR, quasiequilibrium situation prevails
  ⇒ New balance between drift and diffusion
  $np = n_i^2$

Apply $V_{GB}>0$: potential difference across structure increases
⇒ need larger charge dipole
⇒ SCR expands into semiconductor substrate:

Simple way to remember: with $V_{GB}>0$, gate attracts electrons and repels holes.



Qualitatively, physics unaffected by application of $V_{GB} > 0$.
Use mathematical formulation in thermal equilibrium, but:

$$\phi_B \rightarrow \phi_B + V_{GB}$$

For example, to determine $x_d(V_{BG})$:

$$\phi_B + V_{GB} = V_B(V_{GB}) + V_{ox}(V_{GB})$$

$$= \frac{qN_a x_d^2(V_{GB})}{2\varepsilon_s} + \frac{qN_a x_d(V_{GB}) t_{ox}}{\varepsilon_{ox}}$$

$$x_d(V_{GB}) = \frac{\varepsilon_s}{C_{ox}}\left[\sqrt{1+\frac{2C_{ox}^2(\phi_B+V_{GB})}{q\varepsilon_s N_a}}-1\right]$$

$$\phi(0) = \phi_s = \phi_p + \frac{qN_a x_d^2(V_{GB})}{\varepsilon_s}$$

$$V_{GB}\uparrow \rightarrow x_d\uparrow$$

ϕ_s gives n & p concentration at the surface

Summary of Key Concepts

- Charge redistribution in MOS structure in thermal equilibrium
  - SCR in semiconductor
  - ⇒ built in potential across MOS structure.
- In most cases, we can use depletion approximation in semiconductor SCR
- Application of voltage modulates depletion region width in semiconductor
  - ⇒No current flows

MOS Electrostatics(II)

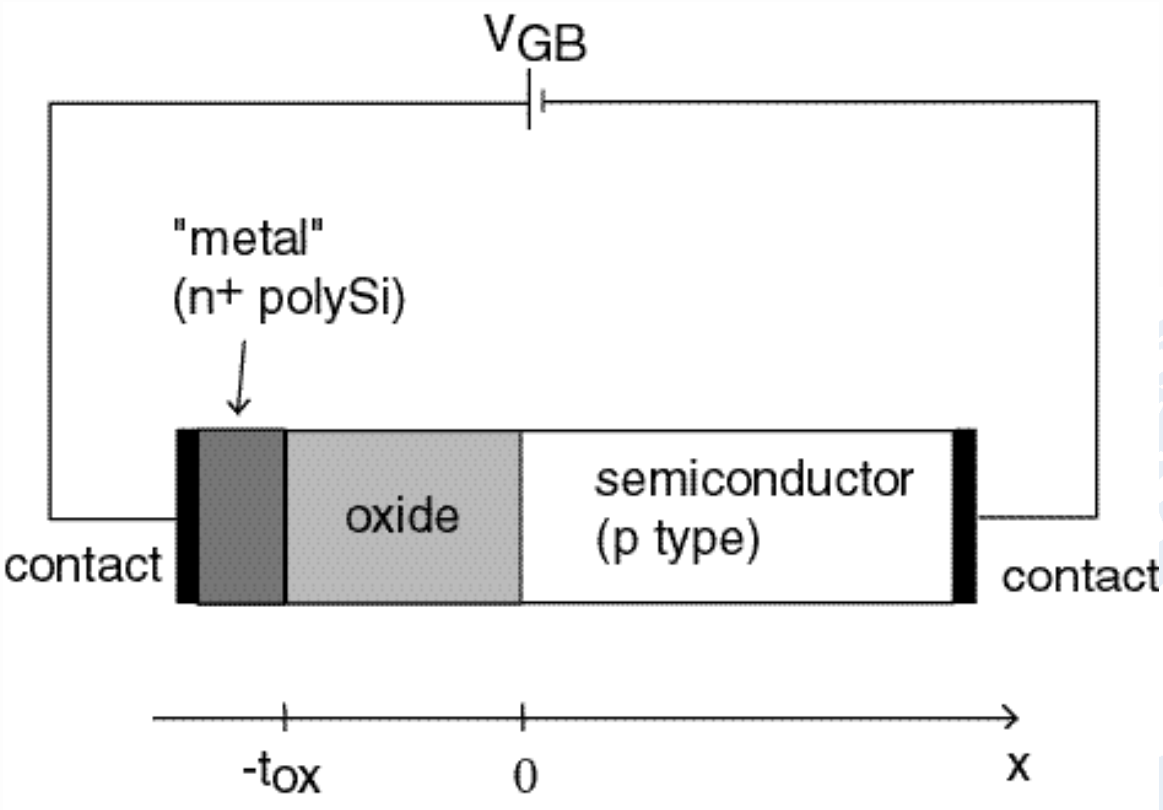
Outline

- Overview of MOS electrostatics under bias
- Depletion regime
- Flatband
- Accumulation regime
- Threshold
- Inversion regime

Key questions

- Is there more than one regime of operation of the MOS structure under bias?
- What does ”carrier inversion” mean and what is the big deal about it?
- How does the carrier inversion charge depend on the gate voltage?

1. Overview of MOS electrostatics under bias



Application of bias:

- **Built-in potential across MOS structure increases from φ_B to $\varphi_B + V_{GB}$**
- **Oxide forbids current flow**
  - **$\Rightarrow$ – $J=0$ everywhere in semiconductor**
    - **– Need drift = diffusion in SCR**
- **Must maintain boundary condition at Si/SiO_2 interface**
  - **$– Eox / Es \approx 3$**

How can this be accommodated simultaneously?

$\Rightarrow$ quasi equilibrium situation with potential build-up across MOS equal to $\varphi_B + V_{GB}$

Important consequence of quasiequilibrium:

⇒ Boltzmann relations apply in semiconductor
[they were derived starting from $J_n = J_p = 0$]

$$n(x) = n_i e^{q\phi(x)/kT}$$

$$p(x) = n_i e^{-q\phi(x)/kT}$$

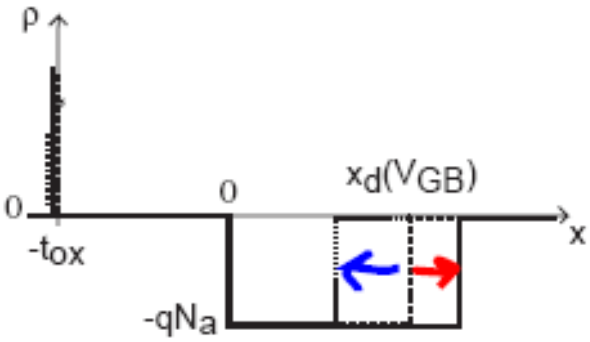
and

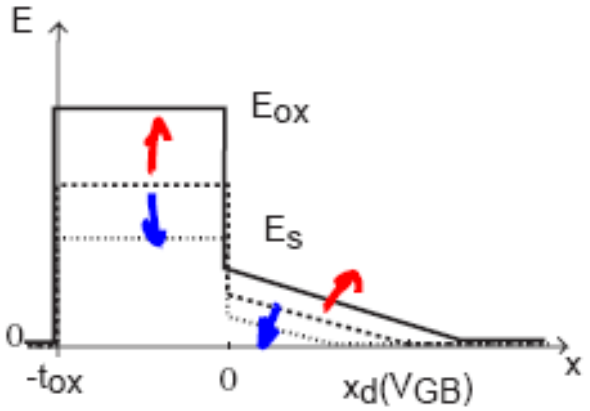
$$np = n_i^2 \qquad \text{at every x}$$

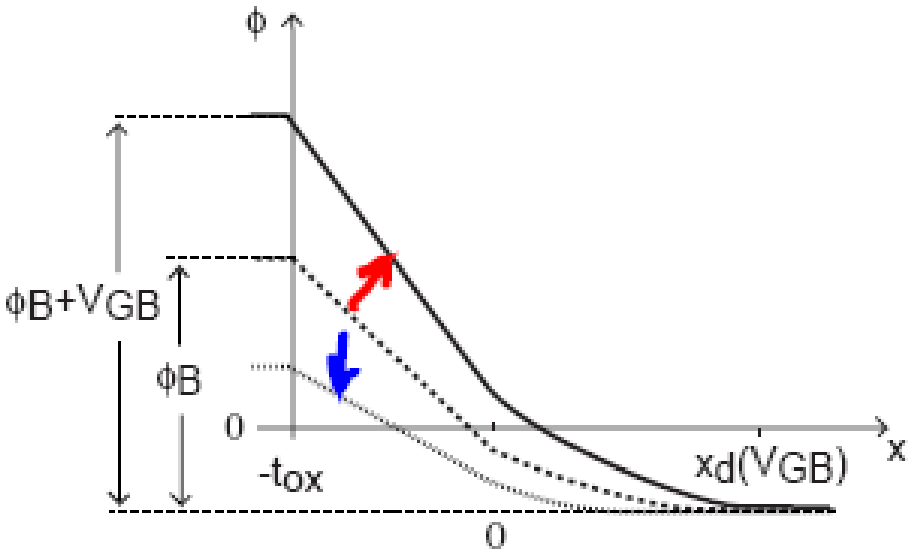
2. Depletion regime

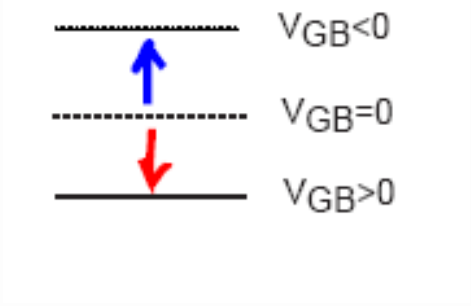
For $V_{GB}>0$, metal attracts electrons and repels holes
⇒ **Depletion region widens**

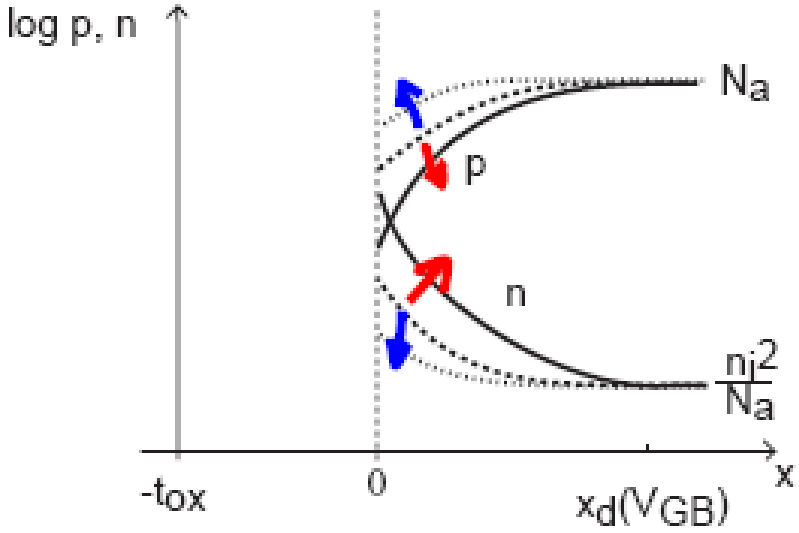
For $V_{GB}<0$, metal repels electrons and attracts holes
⇒ **Depletion region shrinks**


ρ
0
0
xd(VGB)
x
-tox
-qNa


E
Eox
Es
0
-tox
0
xd(VGB)
x


ϕ
ϕB+VGB
ϕB
0
-tox
xd(VGB)
x
0


VGB<0
VGB=0
VGB>0


log p, n
Na
p
n
ni2
Na
-tox
0
xd(VGB)
x

In depletion regime, all results obtained for thermal equilibrium apply if $\varphi_B \rightarrow \varphi_B + V_{GB}$.

Depletion region thickness:

$$x_d(V_{GB}) = \frac{\varepsilon_s}{C_{ox}}\left[\sqrt{1+\frac{2C_{ox}^2(\phi_B + V_{GB})}{\varepsilon_s q N_a}} - 1\right]$$

Potential drop across semiconductor SCR:

$$V_B(V_{GB}) = \frac{qN_a x_d^2}{2\varepsilon_s}$$

Surface potential $\phi(0) = \phi_p + V_B(V_{GB})$

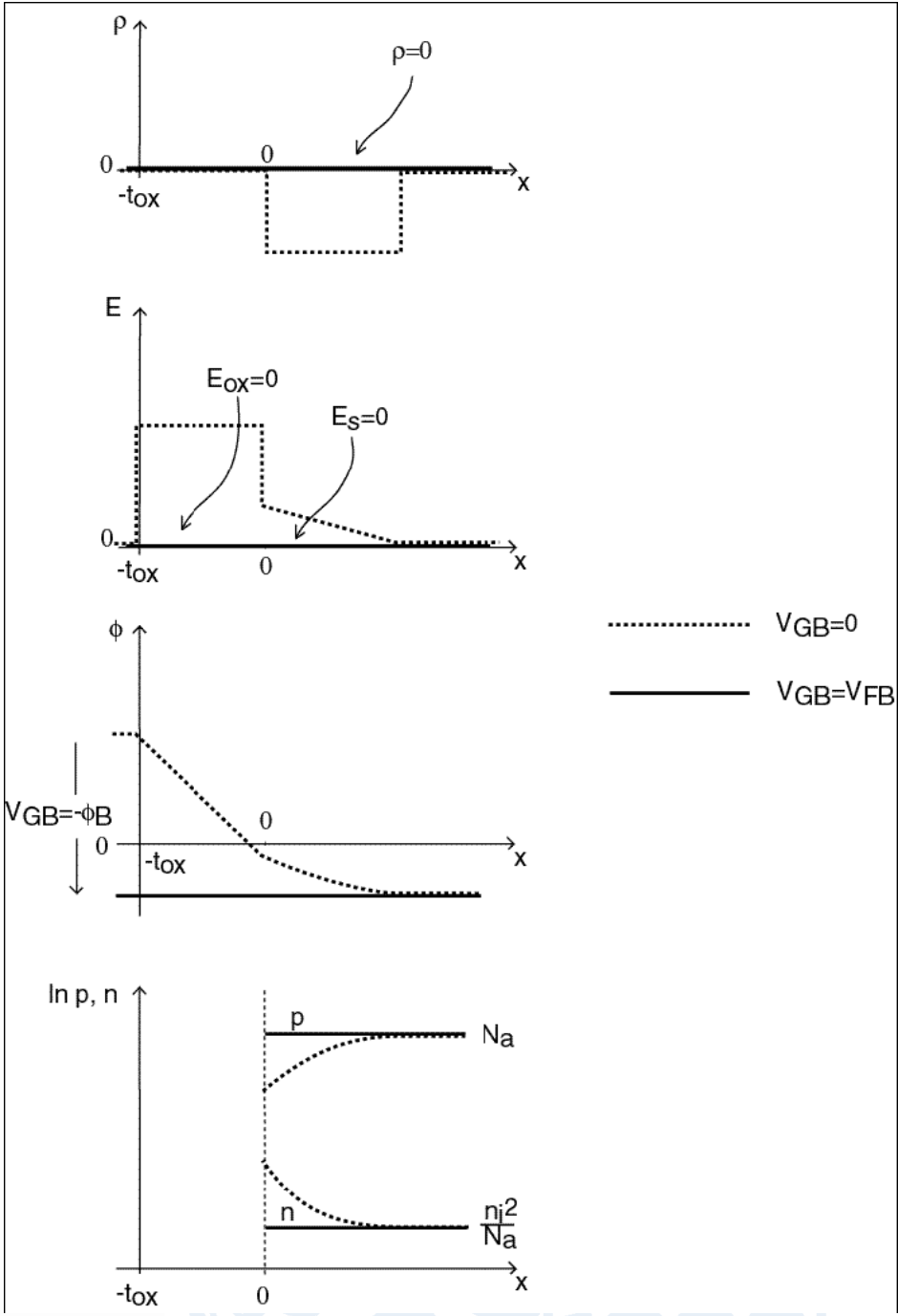
Potential drop across oxide: $V_{ox}(V_{GB}) = \frac{qN_a x_d t_{ox}}{\varepsilon_{ox}}$

3. Flatband

At a certain negative V_{GB}, depletion region is wiped out
⇒ **Flatband**

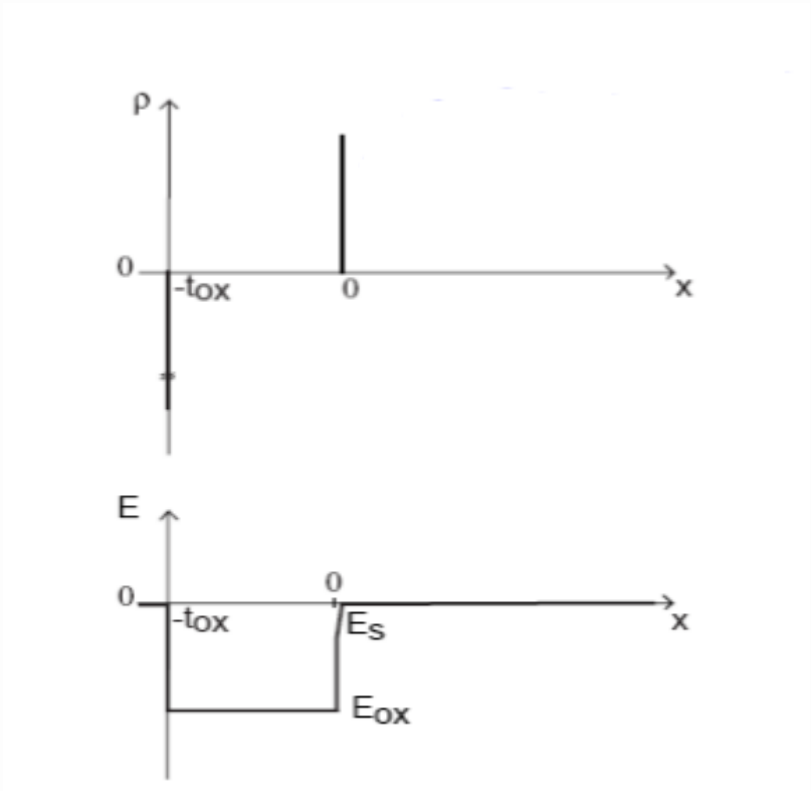
Flatband Voltage:

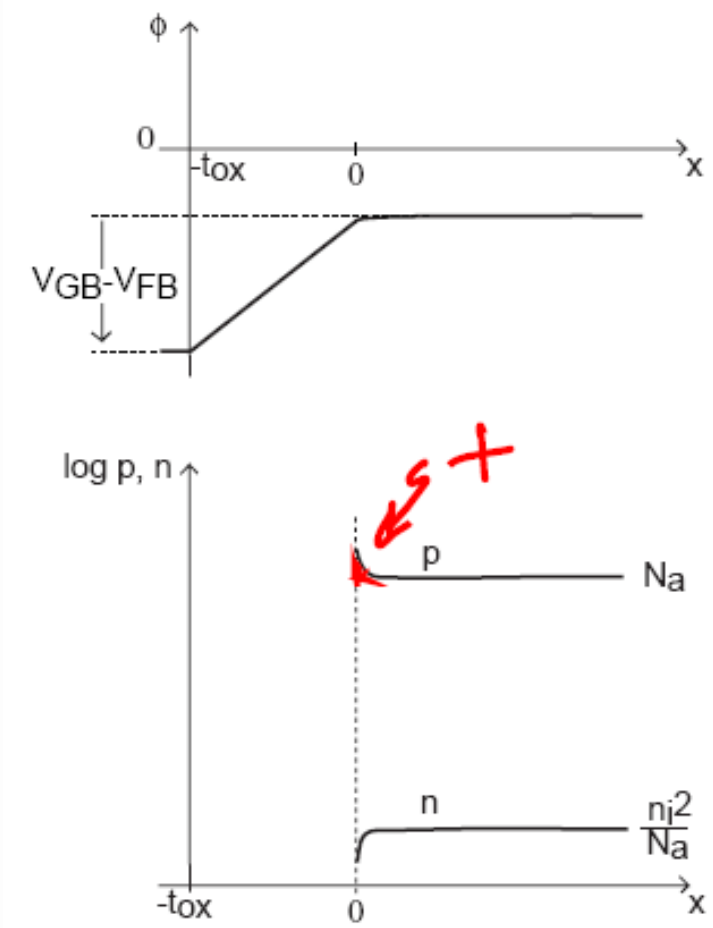
$$V_{GB} = V_{FB} = -\phi_B$$
$$= -(\phi_{N^+} - \phi_p)$$



4. Accumulation regime

If $V_{GB} < V_{FB}$ accumulation of holes at Si/SiO_2 interface



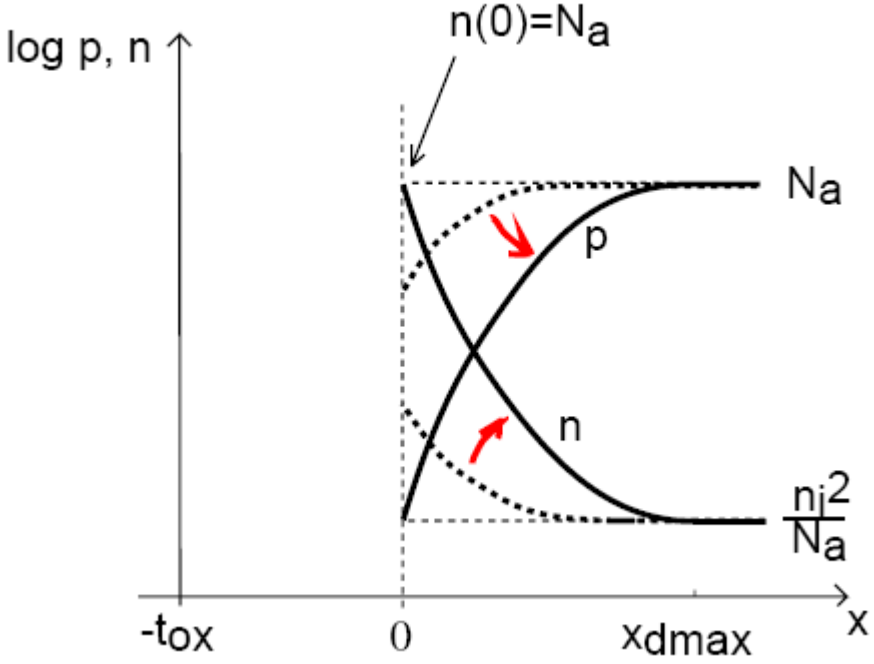


5. Threshold

Back to $V_{GB}>0$.

For sufficiently large $V_{GB} > 0$, electrostatics change when $n(0) = N_a \Rightarrow$ threshold **-Strong Inversion**.

Beyond threshold, cannot neglect contributions of electrons towards electrostatics.



Let's compute the voltage (threshold voltage) that leads to $n(0) = N_a$.

Key assumption: use electrostatics of depletion (neglect electron concentration at threshold).

Computation of threshold voltage.

Three step process:

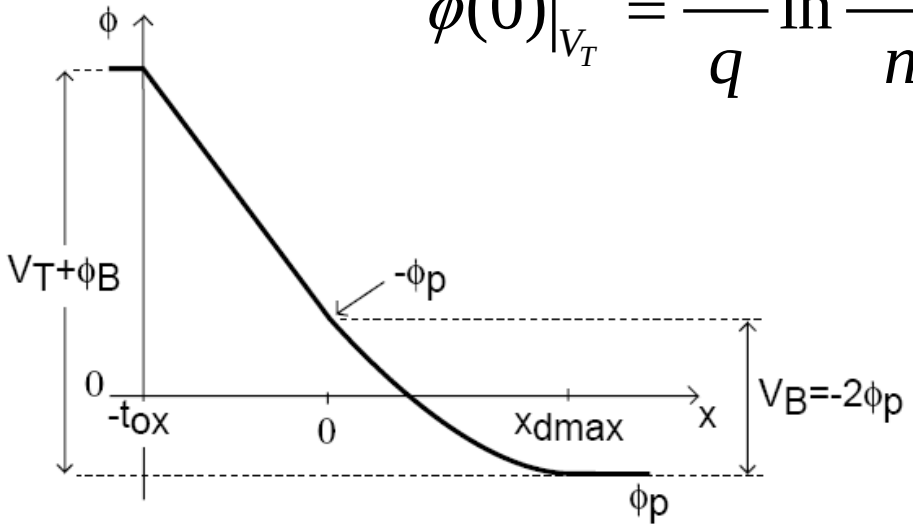
- First, compute potential drop in semiconductor at threshold.

Start from:

$$n(0) = n_i e^{q\phi(0)/kT}$$

$$Solve\ for\ \phi(0)\ at\ V_{GB} = V_T:$$

$$\phi(0)\Big|_{V_T} = \frac{kT}{q}\ln\frac{n(0)}{n_i}\Big|_{V_T} = \frac{kT}{q}\ln\frac{N_a}{n_i} = -\phi_p$$



Hence:

$$V_B(V_T) = -2\phi_p$$

- Second, compute potential drop in oxide at threshold.

Obtain $x_d(V_T)$ using relationship between V_B and x_d in depletion:

$$V_B(V_{GB} = V_T) = \frac{qN_a x_d^2(V_T)}{2\varepsilon_s} = -2\phi_p$$

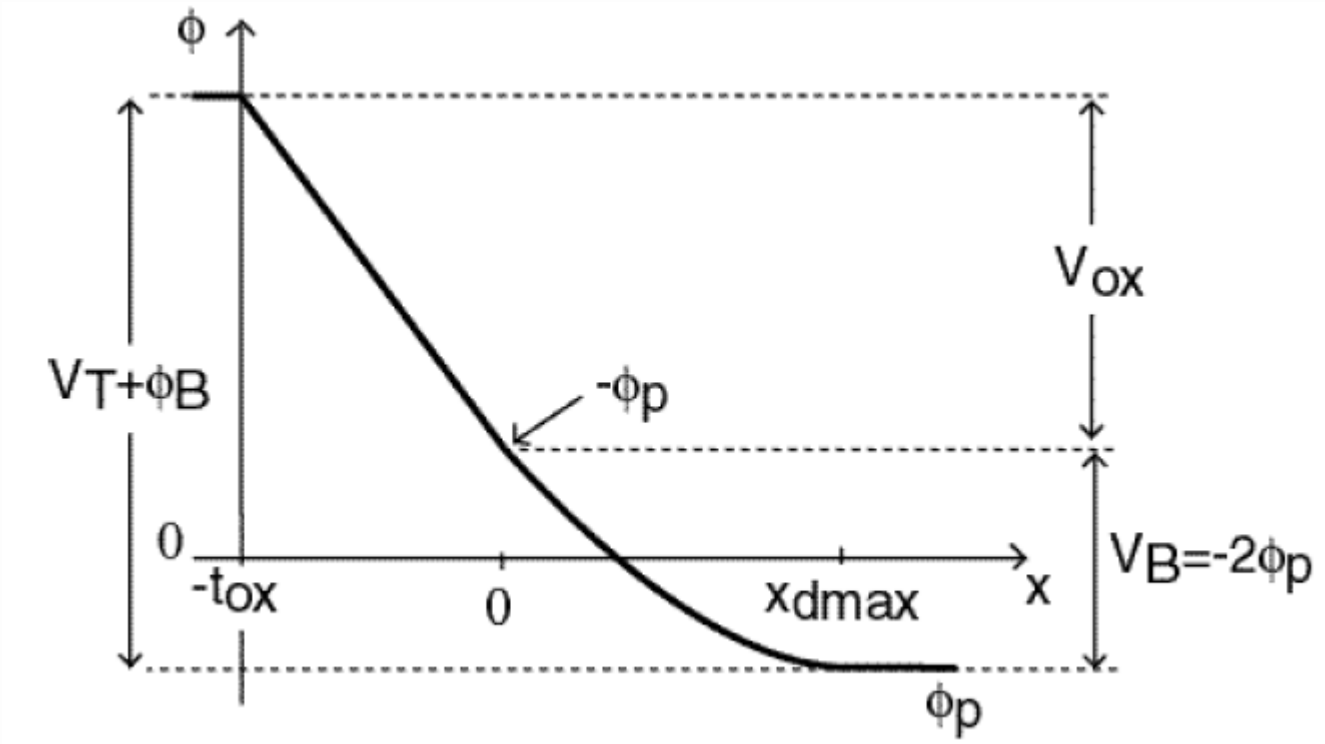
Solve for $x_d(V_T)$:

$$x_d(V_T) = x_{d\max} = \sqrt{\frac{2\varepsilon_s(-2\phi_p)}{qN_a}}$$

Then:

$$V_{ox}(V_T) = E_{ox}(V_T)t_{ox} = \frac{qN_a x_d(V_T)}{\varepsilon_s} t_{ox} = \gamma\sqrt{-2\phi_p}$$

Finally, sum potential drops across structure.



$$V_T + \phi_B = V_B(V_T) + V_{ox}(V_T) = -2\phi_p + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_a(-2\phi_p)}$$

Solve for V_T

$$V_{GB} = V_T = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_a(-2\phi_p)}$$

Key dependencies:

• If $N_a \uparrow \Rightarrow V_T \uparrow$. The higher the doping, the more voltage required to produce *n(0) = Na*

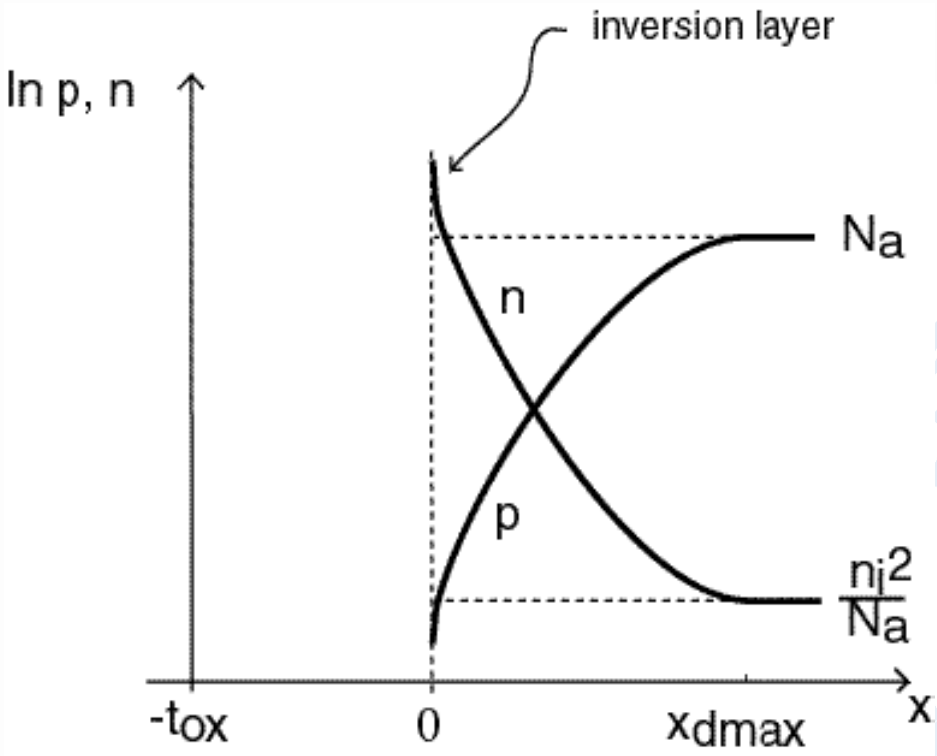
• If *Cox* $\uparrow$ *(tox* $\downarrow$*)* $\Rightarrow V_T \downarrow$. The thinner the oxide, the less voltage dropped across the oxide.

6. Inversion

What happens for $V_{GB} > V_T$?

More electrons at Si/SiO_2 interface than acceptors

⇒ **inversion.**



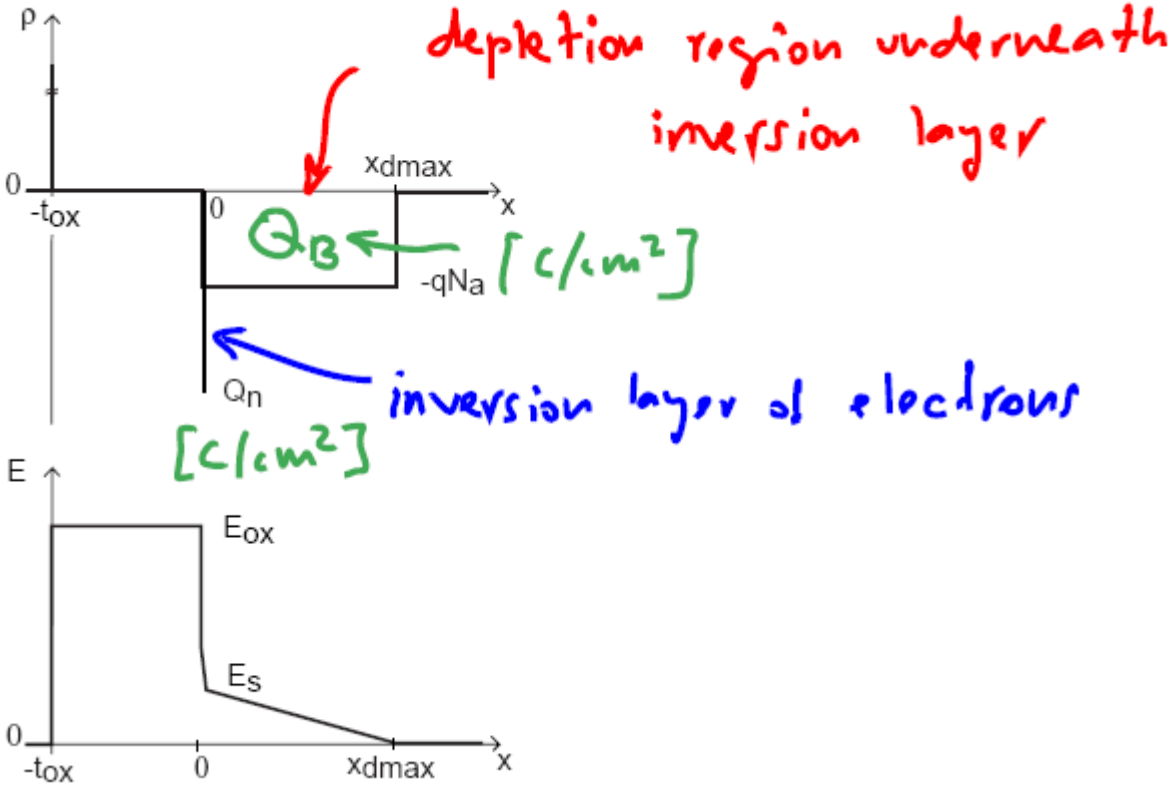
Electron concentration at Si/SiO_2 interface modulated by V_{GB}
$\Rightarrow V_{GB}\uparrow\rightarrow n(0)\uparrow\rightarrow |Q_N|\uparrow$:
Field effect control of mobile charge density!
[essence of MOSFET]

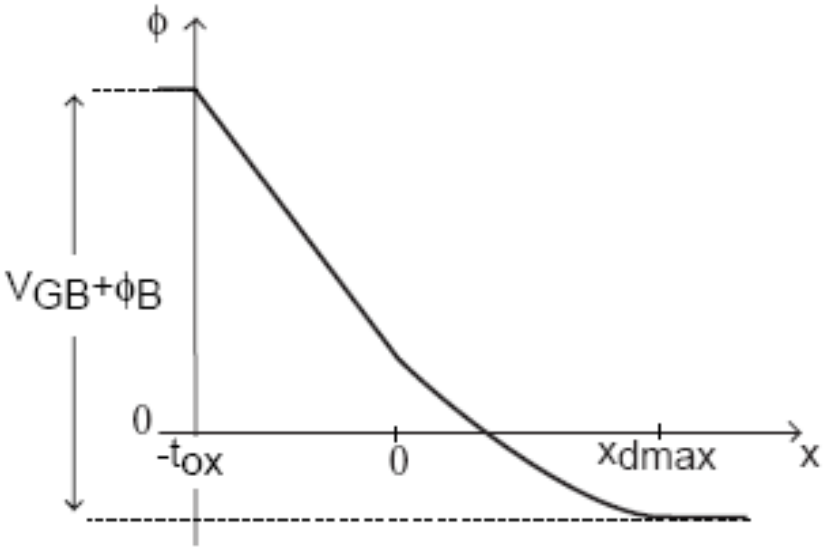
Want to compute Q_N vs. V_{GB} **[charge control relation]**

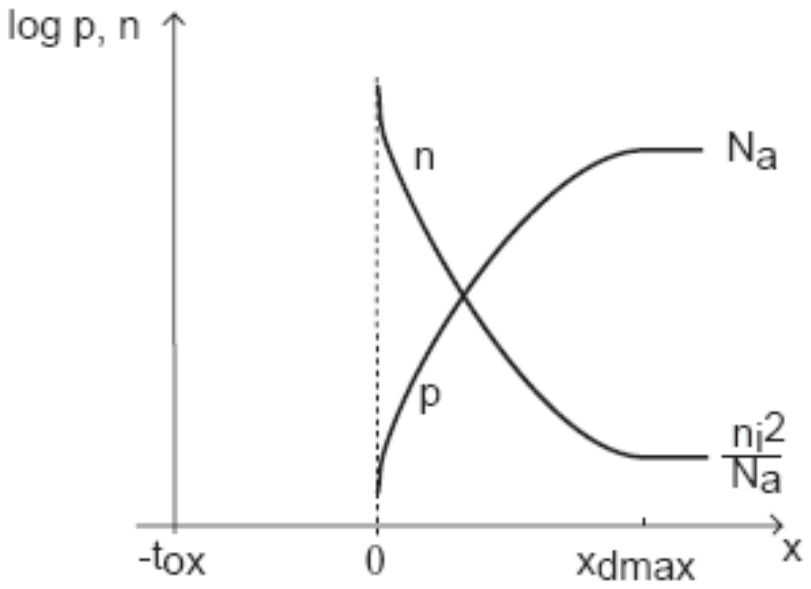
Make sheet charge approximation: electron layer at Si/SiO_2 is much thinner than any other dimension in problem (t_{ox}, x_d).

Charge Control Relation

To derive the charge control relation, let's look at the overall electrostatics:




ϕ
VGB+ϕB
0
-tox
0
xdmax
x


log p, n
n
Na
p
ni2
Na
-tox
0
xdmax
x

Key realization:

$$|Q_n| \propto n(0) \propto e^{q\phi(0)/kT} \qquad n(0) = n_i e^{\frac{q\phi(0)}{kT}}$$

$$|Q_B| \propto \sqrt{\phi(0)} \qquad Q_B = -qN_a x_d \qquad \phi(0) = \phi_s = \phi_p + \frac{qN_a x_d^2(V_{GB})}{2\varepsilon_s}$$

Hence, as $V_{GB}\uparrow$ and $\varphi(0)\uparrow$, $n(0)$ will change a lot, but $|Q_B|$ will change very little.

=> In approximation, Q_B will not increase with V_{GB} when it operates beyond threshold ($V_{GB}>V_T$).

Several consequences:

- x_d does not increase much beyond threshold:

$$\phi_s = -\phi_p \quad \text{In threshold}$$

$$x_d(inv) \approx x_d(V_T) = \sqrt{\frac{2\varepsilon_s(-2\phi_p)}{qN_a}} = x_{d,\max}$$

- V_B does not increase much beyond $V_B(V_T) = -2\varphi_P$ (a thin sheet of electrons does not contribute much to V_B.):

$$V_B(inv) \approx V_B(V_T) = -2\phi_p$$

• All extra voltage beyond V_T used to increase inversion charge Q_n. Think of it as capacitor:

– Top plate: metal gate

– Bottom plate: inversion layer

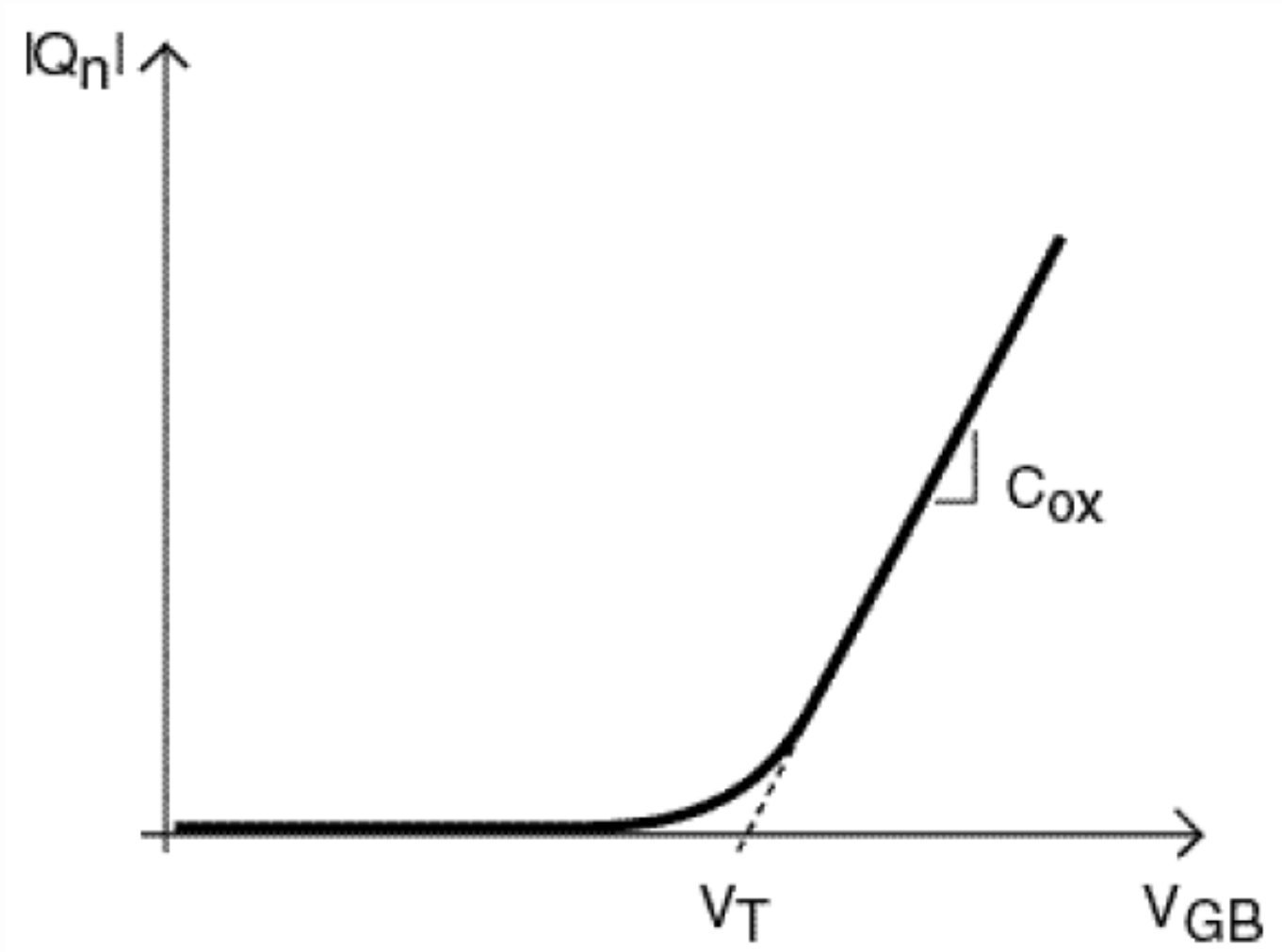
$$Q = CV$$

$$\Rightarrow$$

$$Q_N = -C_{ox}(V_{GB} - V_T) \qquad \text{For } V_{GB} > V_T$$

Though Q_N is not zero for $V_{GB}=V_T$, it is very small as shown in the figure of next page.

Existence of Q_N and control over Q_N by V_{GB}
⇨ Key to MOS electronics


|Qn|
Cox
VT
VGB

上海交通大学
SHANGHAI JIAO TONG UNIVERSITY

MOS Electrostatics(III)

MOS Capacitor

MOS Electrostatics in equilibrium -p type substrate

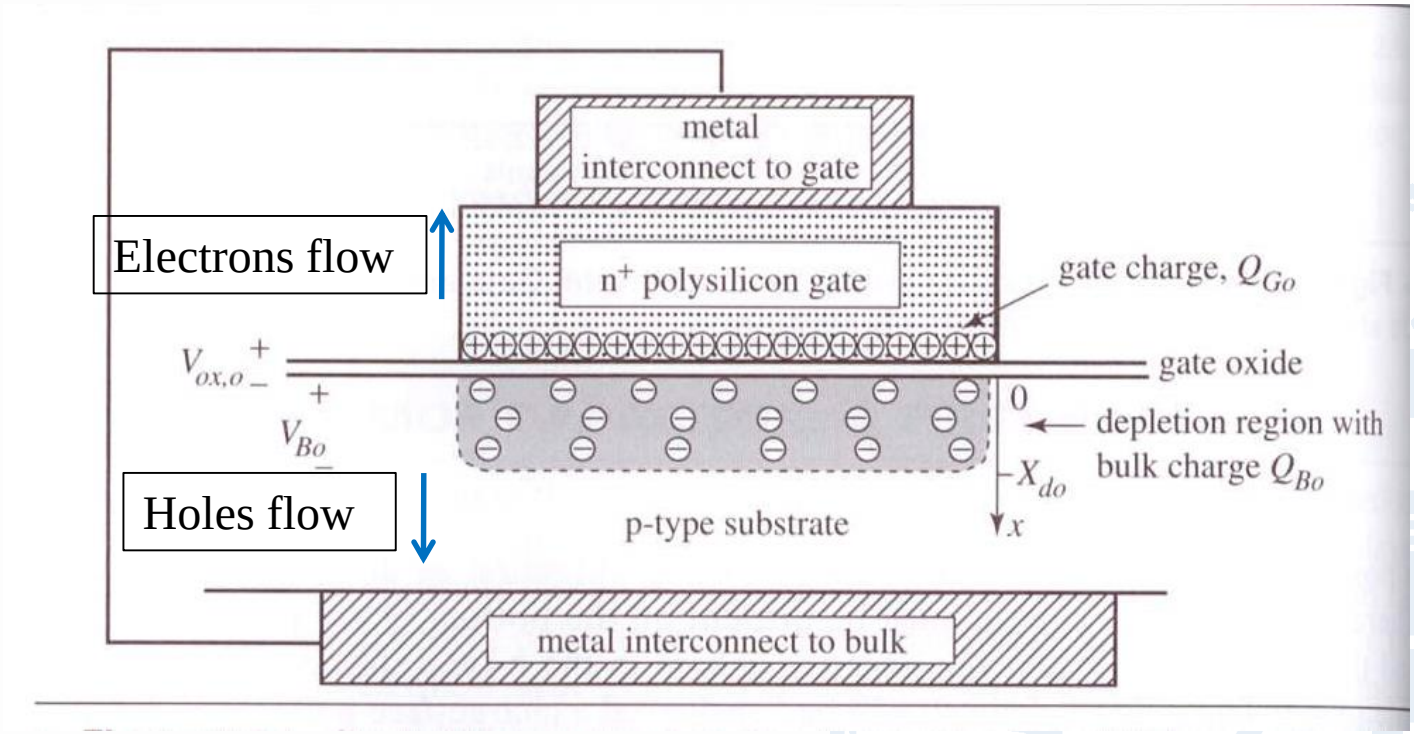
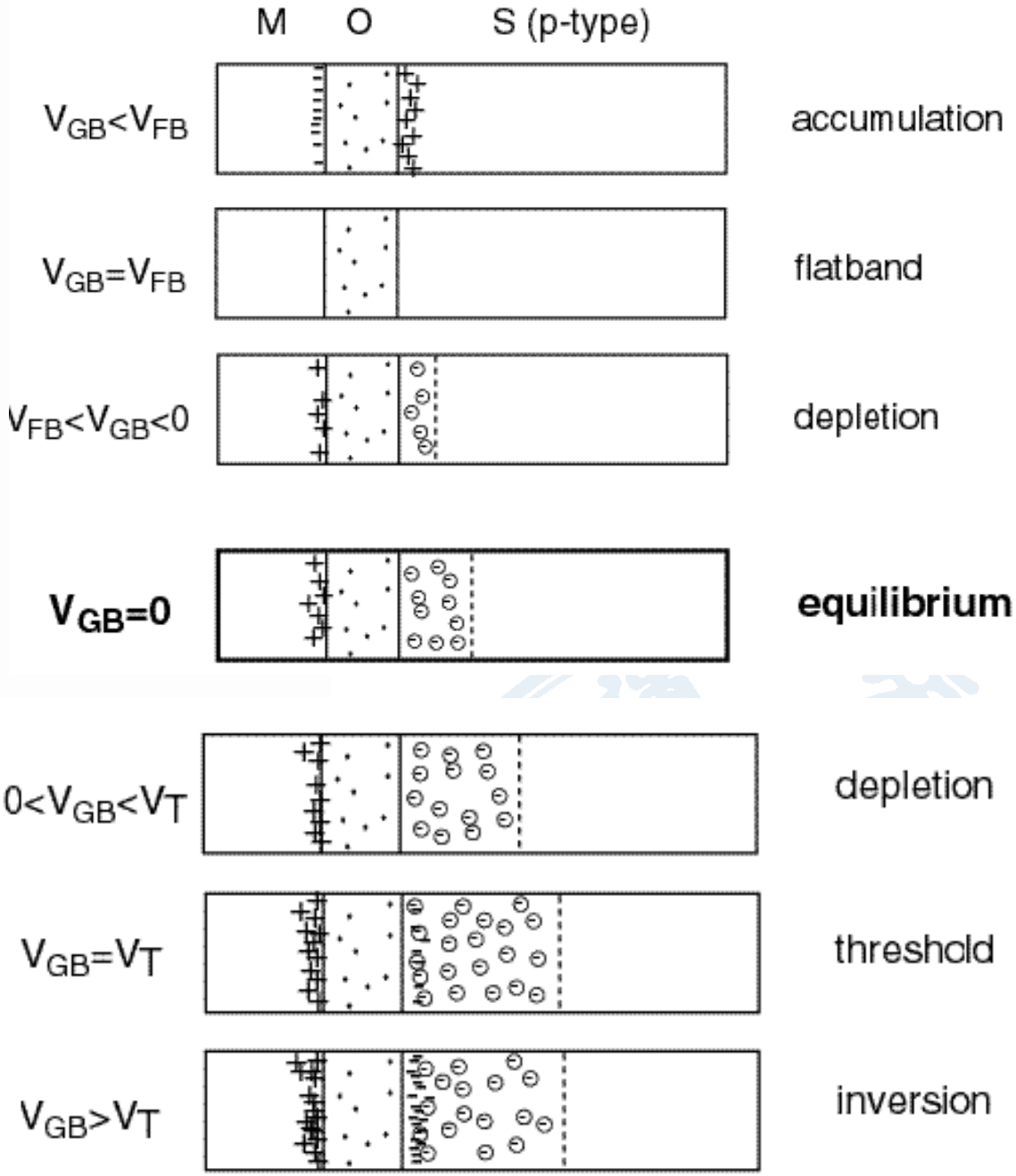


Fig Qualitative picture of charge distribution in an MOS capacitor with p-type substrate in thermal equilibrium.

Operation regimes under bias



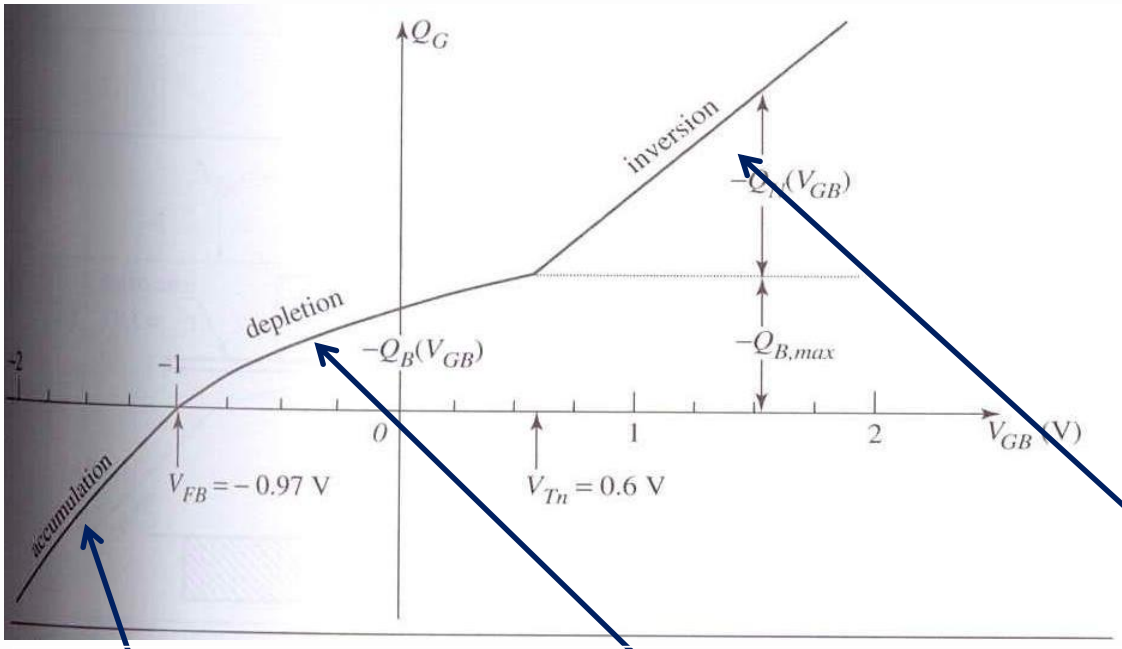


Fig (a) Gate charge as a function of gate-bulk voltage for an MOS capacitor with a *150 Å*-thick gate oxide and a substrate doping $N_a = 10^{17} cm^{-3}$

Gate charge on a p-type substrate

1. Accumulation $(V_{GB} < V_{FB})$

$Q_G = C_{ox}(V_{GB} - V_{FB})$

where $V_{FB} = -(\phi_{N^+} - \phi_p)$

2. Depletion ($V_{FB} < V_{GB} < V_T$)

$$Q_G = -Q_B = qN_a x_d \propto \sqrt{V_{GB}}$$

$$x_d(V_{GB}) = \frac{\varepsilon_s}{C_{ox}}\left[\sqrt{1 + \frac{2C_{ox}^2(\phi_B + V_{GB})}{\varepsilon_s qN_a}} - 1\right]$$

where $V_T = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s qN_a(-2\phi_p)}$

3. Inversion $(V_{GB} > V_T)$

$Q_G = -Q_N(V_{GB}) - Q_{Bmax}$

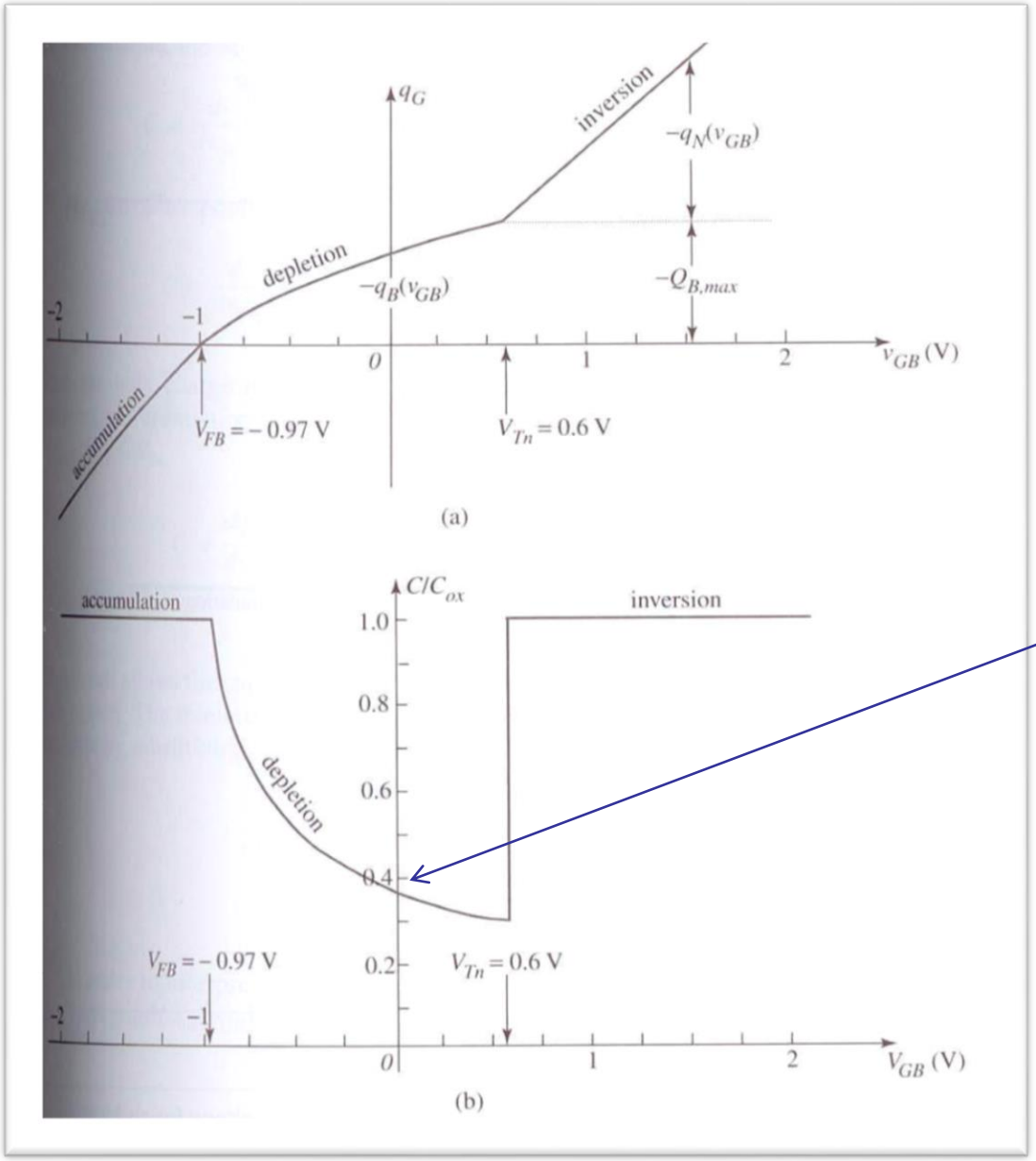
where

$$Q_N = -C_{ox}(V_{GB} - V_T)$$

$$Q_{B\max} = -qN_a x_{d\max}$$

$$x_{d\max} = \sqrt{\frac{2\varepsilon_s(-2\phi_p)}{qN_a}}$$

MOS capacitor on a p-type substrate



Capacitor as the slope of $q_G(V_{GB})$

Fig (a) Gate charge as a function of gate-bulk voltage for an MOS capacitor on a p-type substrate with a *150 Å*-thick gate oxide and a substrate doping $N_a = 10^{17} cm^{-3}$

(b) Capacitance as a function of gate-bulk voltage, found by graphically differentiating (a).

$$Q_G = C_{ox}(V_{GB} - V_{FB}) \quad for \quad V_{GB} \le V_{FB}$$

$$Q_G = -Q_B(V_{GB}) = \frac{q\varepsilon_s N_a}{C_{ox}}\left[\sqrt{1+\frac{2C_{ox}^2(V_{GB}-V_{FB})}{q\varepsilon_s N_a}}-1\right](V_{FB} \le V_{GB} \le V_{Tn})$$

$$Q_G = C_{ox}(V_{GB} - V_{Tn}) + \frac{q\varepsilon_s N_a}{C_{ox}}\left[\sqrt{1+\frac{2C_{ox}^2(V_{Tn}-V_{FB})}{q\varepsilon_s N_a}}-1\right] \quad for \quad V_{Tn} \le V_{GB}$$

Gate charge for:
Accumulation
depletion inversion

$$C = \left.\frac{dq_G}{dv_{GB}}\right|_{V_{GB}}$$

$$C = \frac{d}{dv_{GB}}\left[C_{ox}(v_{GB} - V_{FB})\right]\Big|_{V_{GB} \le V_{FB}} = C_{ox} \quad for \quad V_{GB} \le V_{FB}$$

$$C = \frac{d}{dv_{GB}}\left[C_{ox}(v_{GB} - V_{Tn})\right]\Big|_{V_{Tn} \le V_{GB}} = C_{ox}$$

$$C = \left.\frac{dq_G}{dv_{GB}}\right|_{V_{FB} \le V_{GB} \le V_{Tn}} = \frac{C_{ox}}{\sqrt{1+\frac{2C_{ox}^2(V_{GB}-V_{FB})}{q\varepsilon_s N_a}}}$$

$$C = \left.\frac{dq_G}{dv_{GB}}\right|_{V_{FB}\le V_{GB}\le V_{Tn}} = \frac{C_{ox}}{\sqrt{1+\dfrac{2C_{ox}^2(V_{GB}-V_{FB})}{q\varepsilon_s N_a}}} \qquad x_d(V_{GB}) = \frac{\varepsilon_s}{C_{ox}}\left[\sqrt{1+\frac{2C_{ox}^2(\phi_B+V_{GB})}{\varepsilon_s q N_a}}-1\right]$$

$$C = \frac{C_{ox}}{\left(\dfrac{C_{ox}}{\varepsilon_s}\right)x_d(V_{GB})+1} = \frac{C_{ox}\left(\dfrac{\varepsilon_s}{x_d(V_{GB})}\right)}{C_{ox}+\left(\dfrac{\varepsilon_s}{x_d(V_{GB})}\right)} \quad for \quad V_{FB}\le V_{GB}\le V_{Tn}$$

The capacitance C_b of the depletion region

$$C_b = \frac{\varepsilon_s}{x_d(V_{GB})}$$

$$C = \frac{C_{ox}C_b}{C_{ox}+C_b}$$

In depletion region, MOS capacitor is the capacitances C_{ox} and C_b in series.

MOS Electrostatics in equilibrium n-type substrate

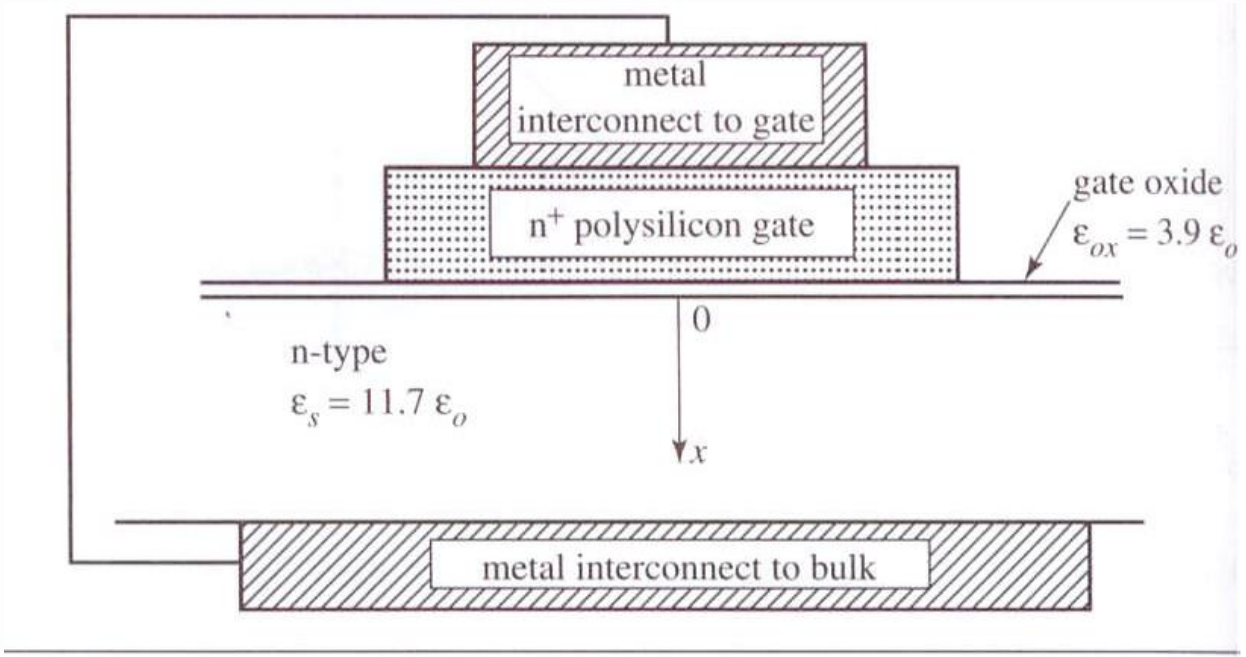


Fig MOS capacitor with n-type substrate. $V_{GB}=0$ for investigate capacitor in thermal equilibrium

Built in potential for $N_d = 10^{17} cm^{-3}$

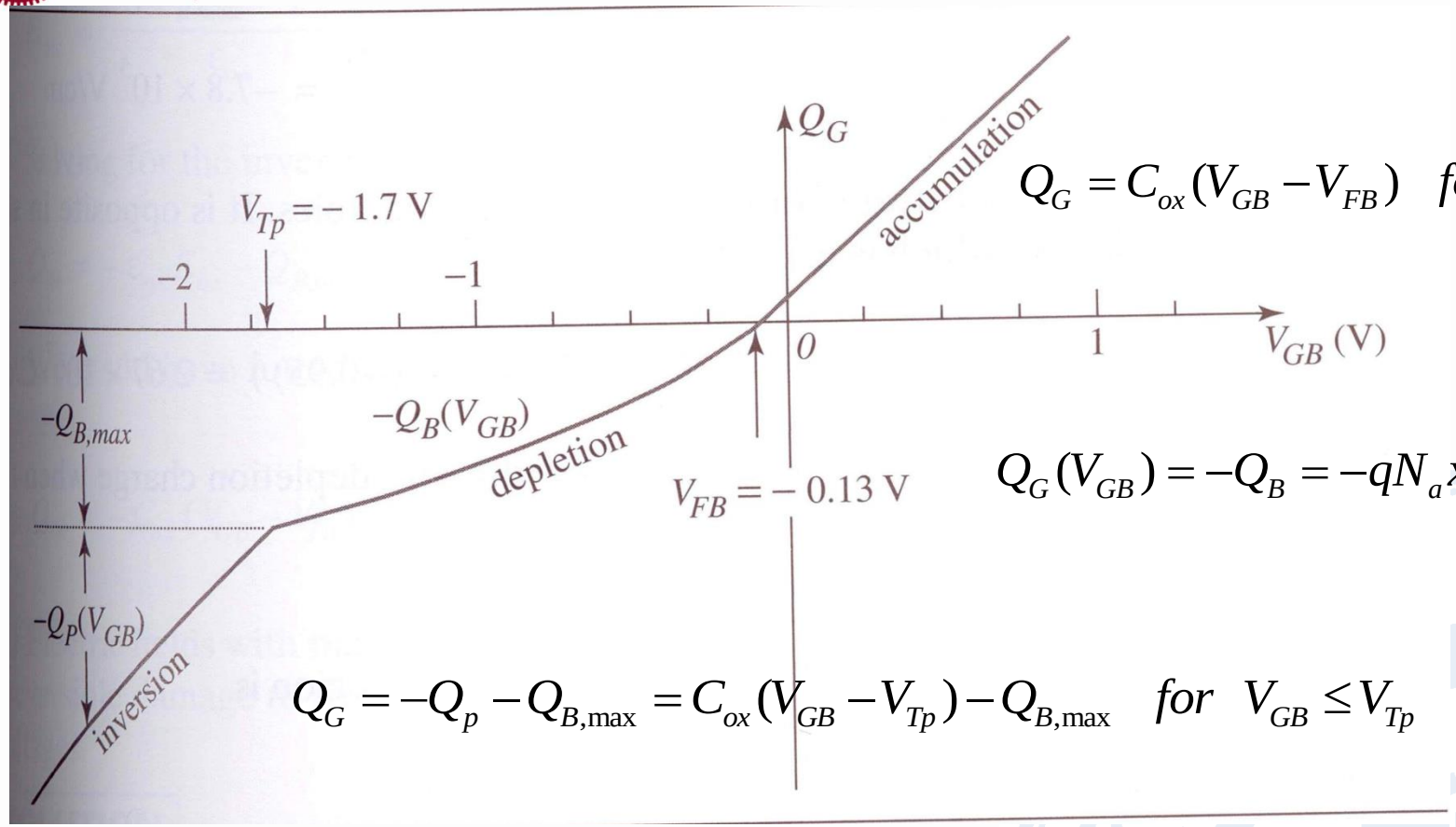
$$\phi_{n^+} - \phi_n = 550mV - 420mV = 130mV$$

Flat band voltage

$$V_{FB} = -(\phi_{n^+} - \phi_n) = -130mV$$

Threshold voltage

$$V_{Tp} = V_{FB} - 2\phi_n - \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_a (2\phi_n)}$$



$$Q_G = C_{ox}(V_{GB} - V_{FB}) \quad for \quad V_{GB} \geq V_{FB}$$

$$Q_G(V_{GB}) = -Q_B = -qN_a x_d(V_{GB})$$

$$Q_G = -Q_p - Q_{B,\max} = C_{ox}(V_{GB} - V_{Tp}) - Q_{B,\max} \quad for \quad V_{GB} \leq V_{Tp}$$

Fig Gate charge as a function of gate-bulk voltage for an MOS capacitor an n-type substrate with doping $N_d = 10^{17} cm^{-3}$ and a *150 Å*–thick gate oxide.

Example 1

Consider a MOS capacitor with $t_{ox}=2 \times 10^{-6}\ cm$ on a p-type substrate with acceptor concentration $N_a=5 \times 10^{16} cm^{-3}$.

a) Find the electric field in the oxide and the charge per unit area in the substrate for V_{GB}=-2.5V.

b) Find the numerical value of the depletion width and depletion charge when the capacitor is biased in the inversion region.

c) Find the electric field in the oxide and the inversion-layer electron charge for V_{GB}=2.5V.

d) Electric fields with magnitudes greater than $E_{ox,max}=5 \times 10^6\ V/cm$ will cause irreversible damage to the gate oxide. Find the permissible rage of gate-bulk voltages.

(A) Solution

The first step is to determine the operation regime (accumulate depletion or inversion regime).

The flatband voltage:

$$V_{FB} = -\phi_B = -(\phi_{n^+} - \phi_p) = -(550mV - 60mV \log \frac{N_a}{n_i})$$

$$= -\left[550mV - (-402mV)\right] = -952mV$$

The threshold voltage:

$$V_{Tn} = V_{FB} - 2\phi_n + \frac{\sqrt{2\varepsilon_s q N_a (-2\phi_p)}}{C_{ox}}$$

We substitute the permittivity of silicon and SiO_2

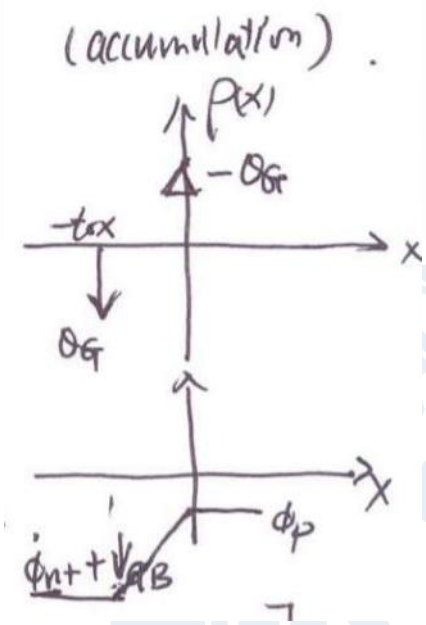
$$\varepsilon_s = 1.04\times10^{-12} F/cm \quad \text{and} \quad \varepsilon_{ox} = 3.45\times10^{-13} F/cm \quad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$V_{Tn} = -0.95V - 2(-0.4V) + \frac{\sqrt{2\times(1.6\times10^{-19}C)\times(1.04\times10^{-12}F/cm)\times(+2\times0.4V)}}{(3.45\times10^{-13}F/cm)/(2\times10^{-6}cm)}$$

$$= -0.95V - 2(-0.4V) + 0.67V = 0.52V$$

Since $V_{GB} = -2.5V < V_{FB} = -0.95V$, MOS operates in accumulation regime. The electric field from the accumulation charge is

$$E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{(V_{GB} + \phi_{n^+}) - \phi_p}{t_{ox}} = \frac{-2.5V + 0.55V - (-0.4V)}{2\times10^{-6}cm} = -7.8\times10^{5}V/cm$$



The charge in the substrate consists of accumulated holes

$$Q_\rho = -Q_G = -C_{ox}(V_{GB} - V_{FB}) = -\frac{3.45\times10^{-13}F/cm}{2\times10^{-6}cm}[-2.5V - (-0.95V)]$$

$$= -1.72\times10^{-7}F/cm^2 \times (-1.55V) = 2.67\times10^{-7}\frac{C/V}{cm^2}V = 2.67\times10^{-7}C/cm^2$$

(B) Solution

In inversion, the potential drop across the depletion region is

$$V_{B,\max} = \phi_s - \phi_p = -\phi_p - \phi_p = -2(-0.4V) = 0.8V$$

Since $V_{B,\max} = \frac{1}{2}\frac{qN_a x_{d\max}^2}{\varepsilon_s}$

$x_{d\max}$ can be solved as:

$$x_{d\max} = \sqrt{\frac{2\varepsilon_s V_{B\max}}{qN_a}} = \sqrt{\frac{2\times 1.04\times 10^{-12}\,F/cm\times 0.8V}{1.6\times 10^{-19}C\times 5\times 10^{16}cm^{-3}}} = 1.44\times 10^{-5}cm$$

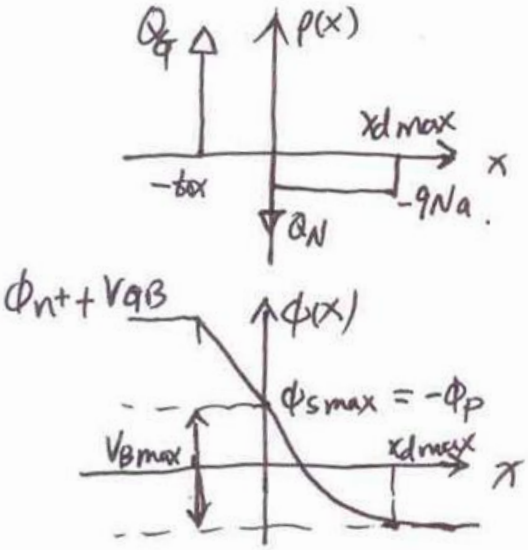
The bulk charge in the depletion region is

$$Q_{B\max} = -qN_a x_{d\max} = -(1.6\times 10^{-19}C)(5\times 10^{-16}cm^{-3})\left(1.44\times 10^{-5}cm\right)$$

$$= -1.15\times 10^{-7}C/cm^2$$

(C) Solution

Since $V_{GB} = 2.5V > V_{Tn} = 0.52V$, MOS operates in inversion regime.



$$E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{(V_{GB} + \phi_{n^+}) - \phi_{s\max}}{t_{ox}} = \frac{(V_{GB} + \phi_{n^+}) - (-\phi_p)}{t_{ox}}$$

$$= \frac{2.5V + 0.55V - (0.4V)}{2\times10^{-6} cm} = 1.32\times10^{6} V/cm$$

Using Gauss's law, we can relate the electric field in the oxide to the substrate charge.

$$E_{ox} = \frac{-(Q_{B\max} + Q_N)}{\varepsilon_{ox}}$$

Solving for the inversion-layer charge, we find

$$Q_N = -\varepsilon_{ox} E_{ox} - Q_{B\max}$$

$$= -3.45\times10^{-13} F/cm \times 1.32\times10^{6} V/cm - (-1.15\times10^{-7} C/cm^2)$$

$$= -3.4\times10^{-7} C/cm^2$$

The inversion layer charge can also be calculated from

$$Q_N = -C_{ox}(V_{GB} - V_{Tn}) = -3.4\times10^{-7} C/cm^2$$

(D) Solution

In accumulation, the electric field in the oxide is

$$E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{(V_{GB} + \phi_{n^+}) - \phi_p}{t_{ox}}$$

Solving for the most negative gate-bulk voltage using

$E_{ox} = -5 \times 10^{-6} V / cm$, we find that

$$V_{GB,\min} = E_{ox} t_{ox} - \phi_{n^+} + \phi_p$$

$$= (-5 \times 10^{-6} V / cm)(2 \times 10^{-6} cm) - 0.55V + (-0.4V) = -10.95V$$

In inversion, the electric field in the oxide is

$$E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{(V_{GB} + \phi_{n^+}) - (-\phi_p)}{t_{ox}}$$

Substituting the maximum positive field

$E_{ox} = 5 \times 10^{-6} V / cm$, we find that

$$V_{GB,\max} = E_{ox} t_{ox} - \phi_{n^+} - \phi_p$$

$$= (5 \times 10^{-6} V / cm)(2 \times 10^{-6} cm) - 0.55V - (-0.4V) = 9.05V$$

Example 2

Given a MOS capacitor on an n-type substrate with an n^+ poly gate($\phi_{n+} = 550\text{mV}$), a donor concentration N_d=10^{16} cm^{-3}, and an oxide thickness t_{ox}=5x10^{-6} cm. the contact potentials have values $\phi_{mn+} = -400\text{mV}$ $\phi_{nm} = 210\text{mV}$

a) Find the flatband voltage V_{FB}

b) Plot the potential distribution in thermal equilibrium

c) Find the threshold voltage V_{Tp}

d) Plot the potential for V_{GB}=V_{TP}.

(A) Find the flatband voltage V_{FB}

Solution

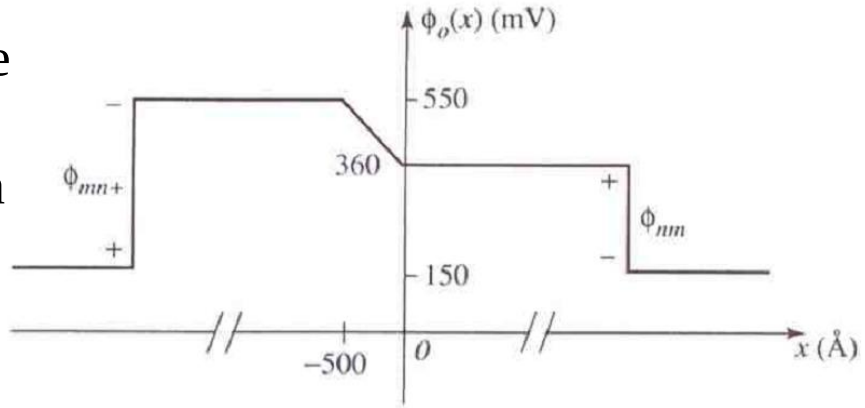
The flatband voltage is equal and opposite to the built-in voltage in the MOS structure

$$V_{FB} = -(\phi_{n^+} - \phi_n) = -(550mV - 360mV) = -190mV$$

(B) Plot the potential $\phi_0(x)$ in thermal equilibrium

Solution

The MOS capacitor is accumulated in thermal equilibrium, since accumulate electrons under the gate balance the positive gate charge. We can sketch the potential since the substrate charge is a delta function at the SiO_2 silicon interface with value Q_{NO}=-Q_{GO}, as shown in the figure.



(C) Find the threshold voltage V_{Tp}

Solution

In order to invert the surface, we must first apply V_{FB} to reach flatband. To deplete the substrate, we must apply $V_{GB}<V_{FB}$ to repel the mobile electrons from the surface and leave the positively charged ionized donors. At the onset of inversion, the surface potential will be lowered to the point where it is equal and opposite to that of the n-type bulk: $\phi_s^{'} = -\phi_n$. Adding the flatband voltage, the voltage drop across the depletion region $V_B^{'} = V_{B,\max} = -2\phi_n$ and the voltage drop across the oxide$V_{ox}^{'}$ the threshold voltage V_{Tp} is

$$V_{Tp} = V_{FB} - 2\phi_n + V_{ox}^{'} = V_{FB} - 2\phi_n - \frac{Q_{B,\max}}{C_{ox}}$$

Note that the drop across the oxide is negative since the substrate has a positive depletion charge $Q_{B,max}>0$ and the gate charge is negative. Substituting for the maximum depletion charge $Q_{B,max}$ .we find

$$V_{Tp} = V_{FB} - 2\phi_n - \frac{\sqrt{2\varepsilon_s q N_d (2\phi_n)}}{C_{ox}} = -0.19 - 0.72 - \frac{4.88\times10^{-8} C/cm^2}{6.9\times10^{-8} F/cm} = -1.62V$$

(D)Plot the potential $\phi(x)$ *for* $V_{GB} = V_{Tp}$

Solution

When $V_{GB}=V_{Tp}$=-1.62V, the n^+ polysilicon gate has a potential of *0.55-1.62=-1.07V*. The potential in the n-type bulk remains fixed at $\phi_n = 0.36V$ with the surface potential at the onset of inversion $\phi_s = -\phi_n = -0.36V$. The potential varies quadratically in the depletion region, which has a width

$$x_{d,\max} = \sqrt{\frac{2\varepsilon_s(2\phi_n)}{qN_a}} = \sqrt{\frac{2 \bullet 11.7 \bullet 8.85\times10^{-14} \bullet 0.72}{1.6\times10^{16}}} = 0.31\mu m$$

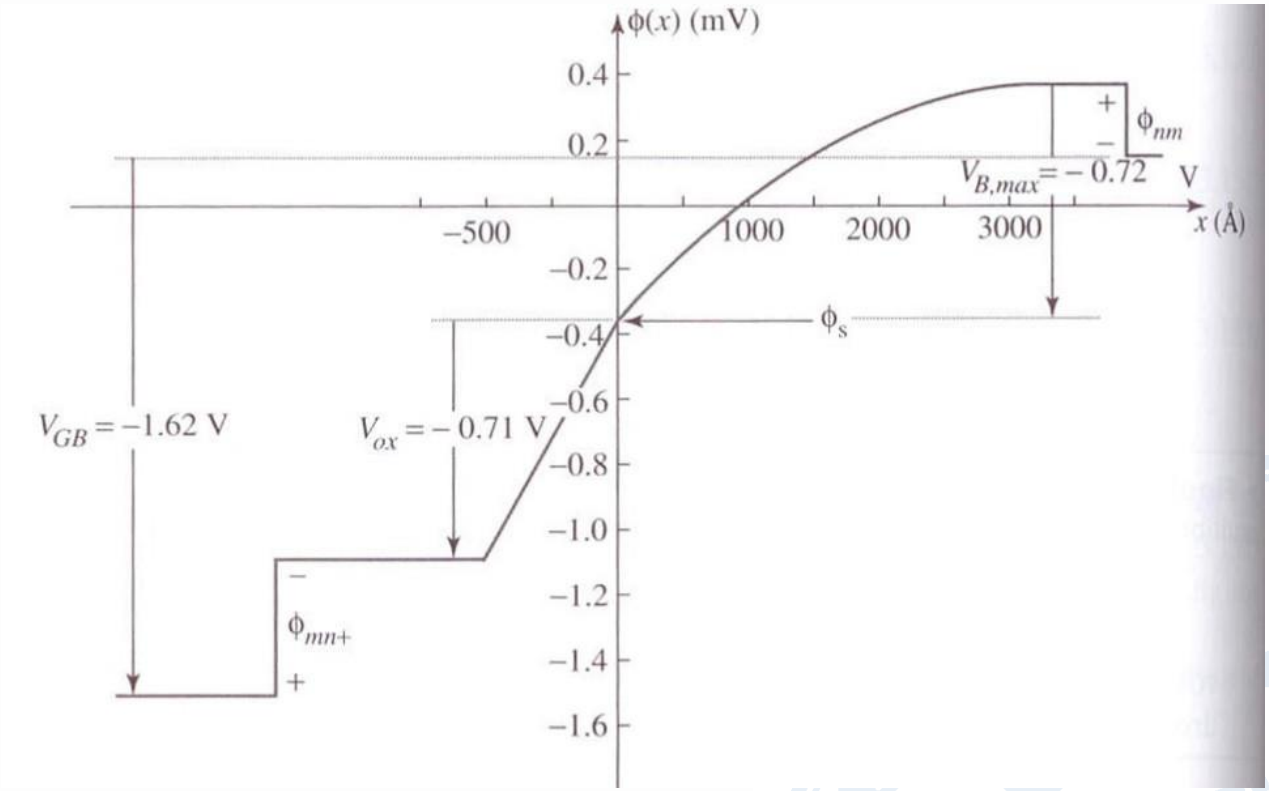


Fig Potential of MOS structure with n-type substrate for the case where $V_{GB}=V_{Tp}$.

Homework 14

Consider a MOS capacitor with $t_{ox}=2 \times 10^{-6}\ cm$ on a p-type substrate with acceptor concentration $N_a=5 \times 10^{16} cm^{-3}$.

（a）Compute and plot the MOS capacitance versus V_{GB}.

(b) Compute and plot the gate charge versus V_{GB}.