Lecture 14

MOSFET I-V CHARACTERISTICS

Outline

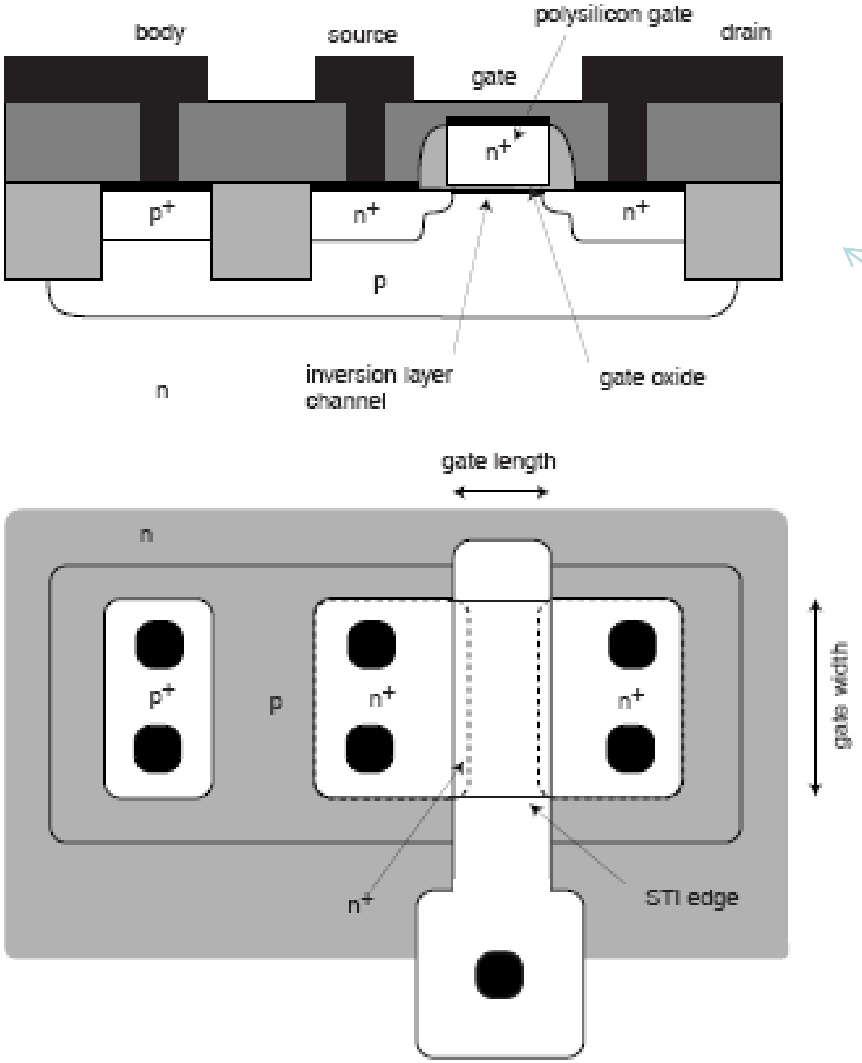
1. MOSFET: cross-section, layout, symbols
2. Qualitative operation
3. *I-V* characteristics

Key questions

- How can carrier inversion be exploited to make a transistor?
- How does a MOSFET work?
- How does one construct a simple first-order model for the current-voltage characteristics of a MOSFET?

1. MOSFET:

layout, cross-section, platform



Shallow trench isolation (STI)

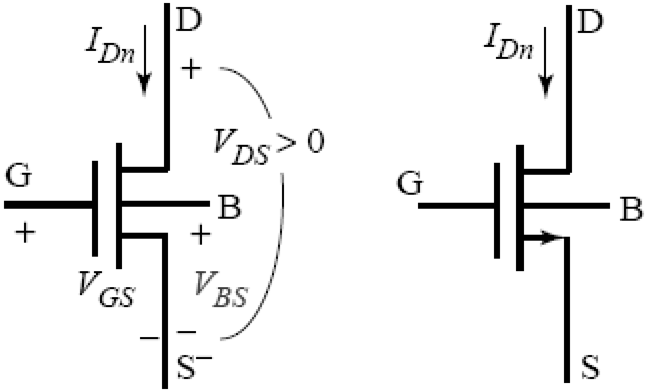
Key elements:

- inversion layer under gate (depending on gate voltage)
- heavily-doped regions reach underneath gate =->inversion layer electrically connects source and drain
- 4-terminal device: body voltage important

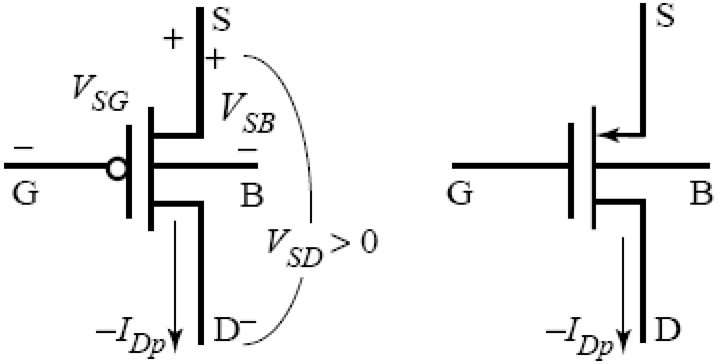
Circuit symbols

Two complementary devices:

- **n-channel device (n-MOSFET) on p-substrate**
  - **uses electron inversion layer**
- **p-channel device (p-MOSFET) on n-substrate**
  - **uses hole inversion layer**



(a) n-channel MOSFET



(b) p-channel MOSFET

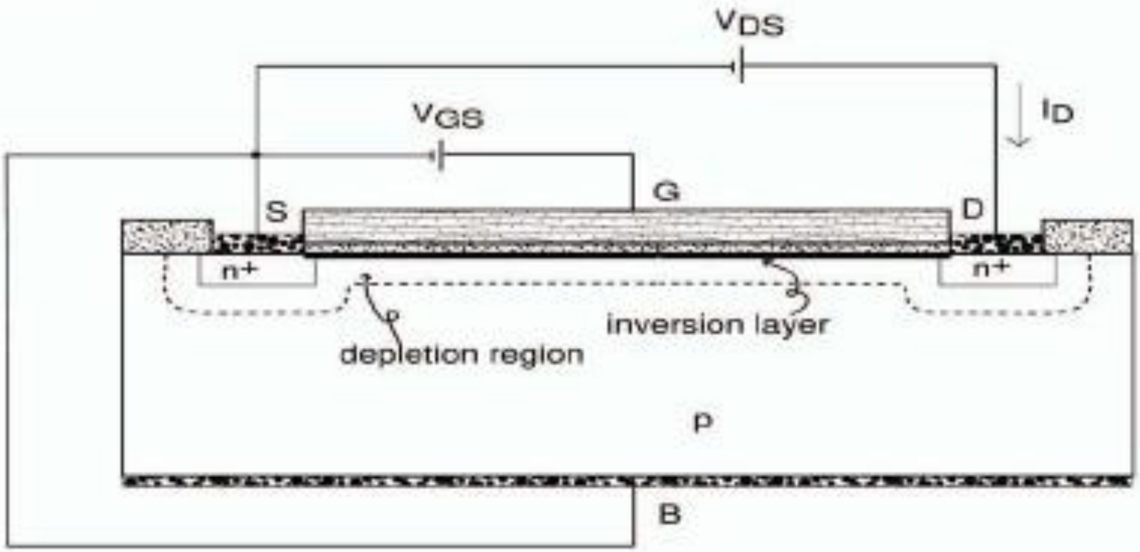
Qualitative Operation

- ***Drain Current*** (I_d: proportional to inversion charge and the velocity that the charge travels from source to drain

- ***Velocity :***proportional to electric field from drain to source

- ***Gate-Source Voltage*** (V_{GS} controls amount of inversion charge that carries the current

- ***Drain-Source Voltage*** (V_{DS}: controls the electric field that drifts the inversion charge from the source to drain

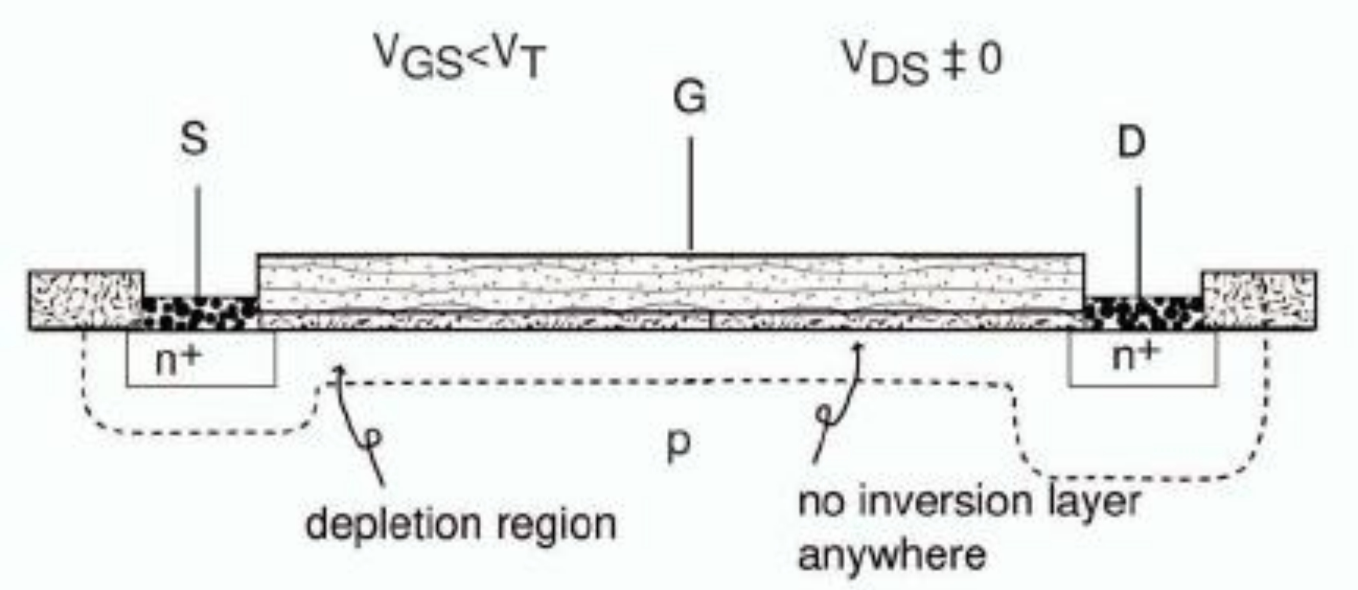


Want to understand the relationship between the drain current in the MOSFET as a function of gate-to-source voltage and drain-to-source voltage.

Initially consider source tied up to body (substrate)

Three regimes of operation:

- MOSFET:
  -$V_{GS}<V_T$, with $V_{DS}\geq 0$
- Inversion Charge=0
- V_{DS} drops across drain depletion region
- $I_D=0$



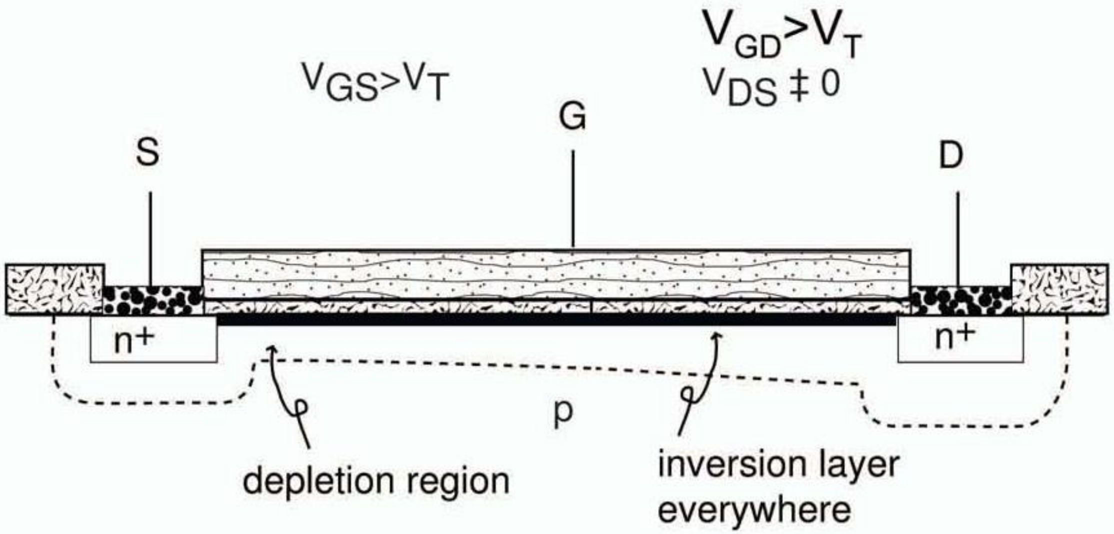
Linear or Triode regime:

Electrons drift from source to drain →electrical current!

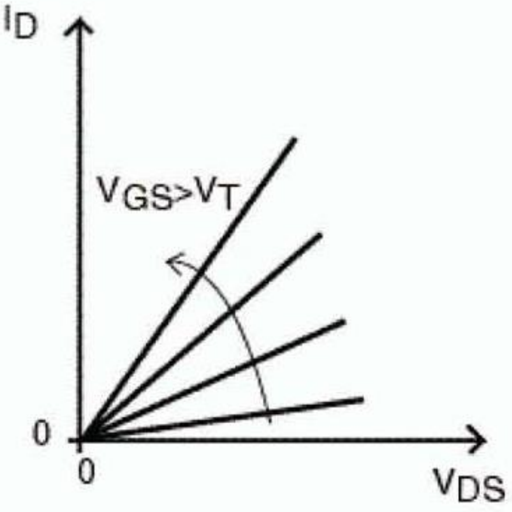
$$V_{GS}\uparrow\Rightarrow|Q_N|\uparrow\Rightarrow I_D\uparrow$$

$$V_{DS}\uparrow\Rightarrow E_y\uparrow\Rightarrow I_D\uparrow$$

$$V_{DS}\ll V_{GS}-V_T$$



$$V_{GD}=V_{GS}-V_{DS}$$

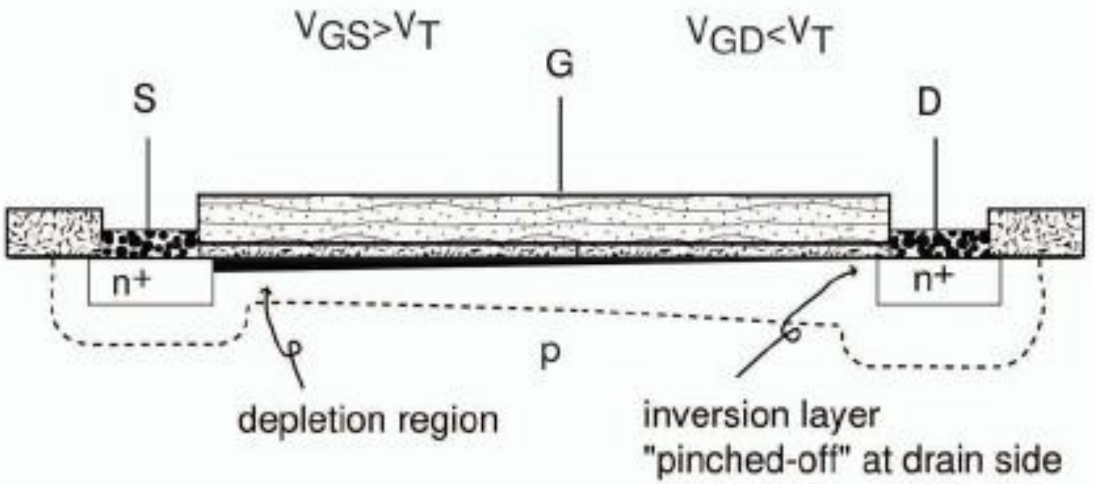


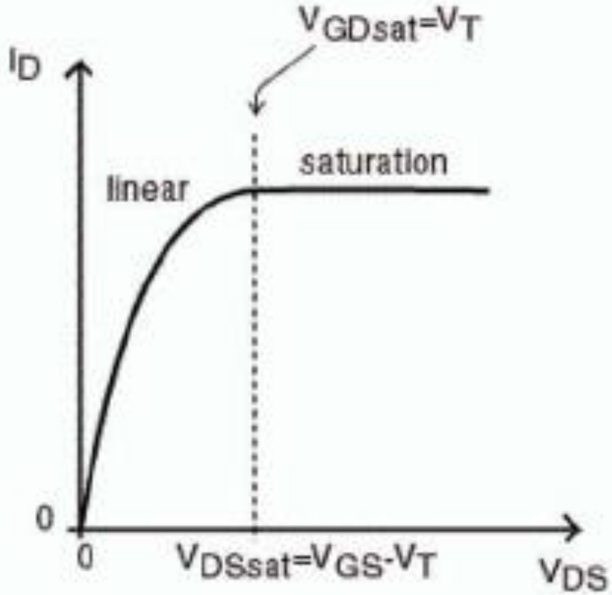
Saturation Region $V_{DS} > V_{GS} - V_T$

$$V_{GS} > V_T, V_{GD} < V_T \Rightarrow V_{DS} > V_{GS} - V_T$$

I_D is independent of V_{Ds}: $I_D = I_{dsat}$

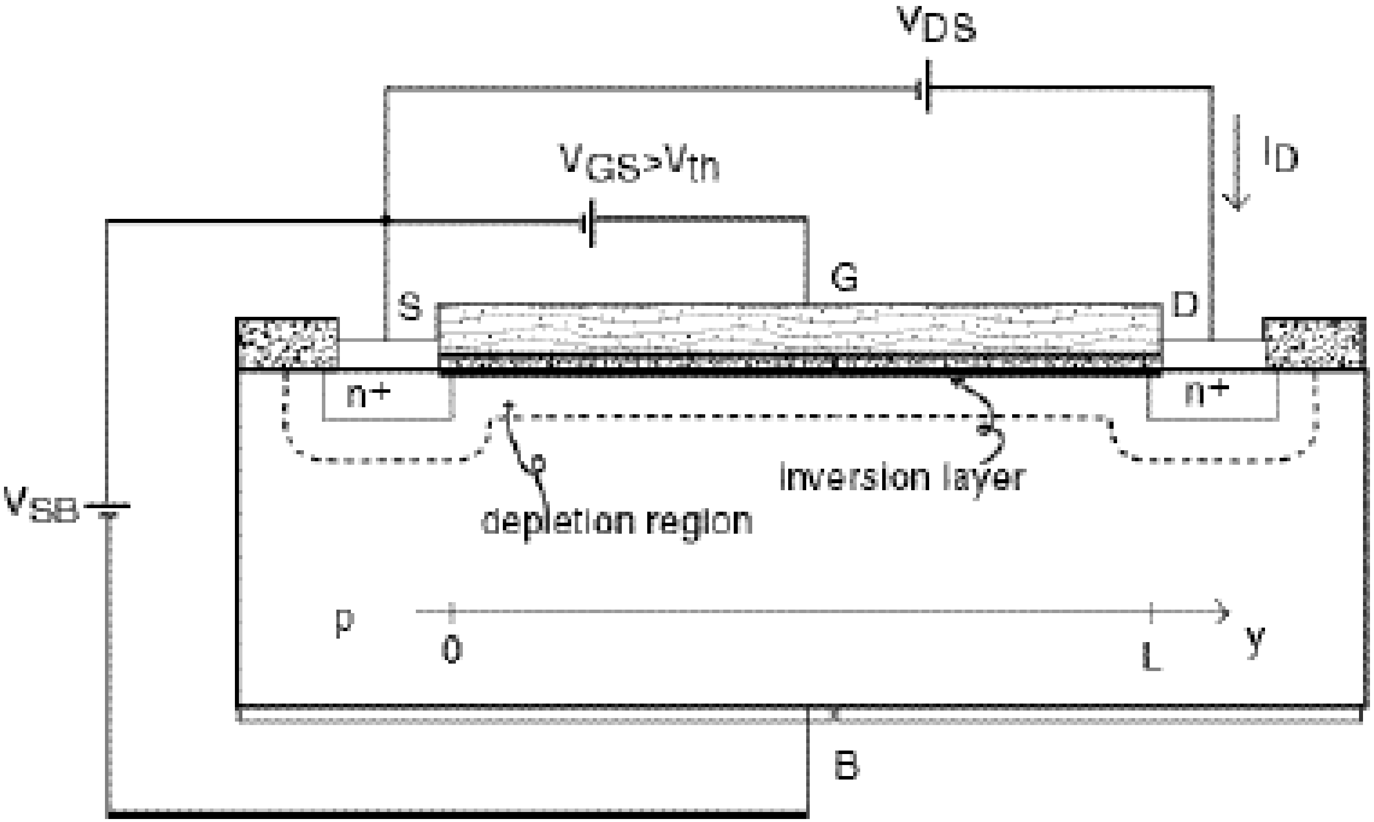
Electric field in channel cannot increase with V_{Ds}





3. *I-V* Characteristics (Assume $V_{SB}=0$)

Geometry of problem:



General expression of channel current

Current can only flow in the y-direction, Total channel flux:

$$I_y = W \bullet Q_N(y) \bullet v_y(y)$$

Drain current is equal to minus channel current:

$$I_D = -W \bullet Q_N(y) \bullet v_y(y)$$

Rewrite in terms of voltage at channel location *y*, *V(y):*

- If electric field is not too high (velocity saturation doesn't occur):

$$v_y(y) = -\mu_n \bullet E_y(y) = \mu_n \bullet \frac{dV}{dy}$$

- For $Q_N(y)$, use charge-control relation at location y:

$$Q_N(y) = -C_{ox}\left[V_{GS} - V(y) - V_T\right]$$

$$for \quad V_{GS} - V(y) \geq V_T$$

All together the drain current is given by:

$$I_D = W \bullet \mu_n C_{ox} \left[V_{GS} - V(y) - V_T \right] \bullet \frac{dV(y)}{dy}$$

Solve by separating variables:

$$I_D d_y = W \bullet \mu_n C_{ox} \left[V_{GS} - V(y) - V_T \right] \bullet dV$$

Integrate along the channel in the linear regime subject the boundary conditions :

Then:

$$I_D \int_0^L dy = W \bullet \mu_n C_{ox} \int_0^{V_{DS}} \left[V_{GS} - V(y) - V_T \right] \bullet dV$$

Resulting in:

$$I_D\left[y\right]_0^L = I_D L = W\bullet\mu_n C_{ox}\left[\left(V_{GS}-\frac{V}{2}-V_T\right)V\right]_0^{V_{DS}}$$

$$\boxed{I_D = \frac{W}{L}\bullet\mu_n C_{ox}\left[V_{GS}-\frac{V_{DS}}{2}-V_T\right]\bullet V_{DS}}$$

$$for \quad V_{DS} < V_{GS} - V_T$$

For small V_{DS}:

$$I_D \simeq \frac{W}{L}\mu_n C_{ox}\left(V_{GS}-V_T\right)V_{DS}$$

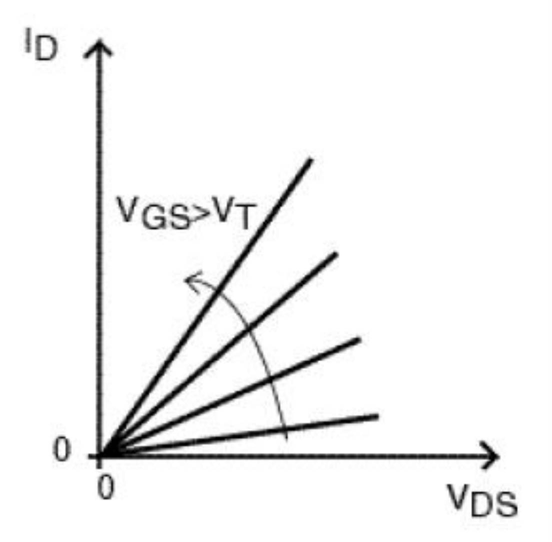
Key dependencies:

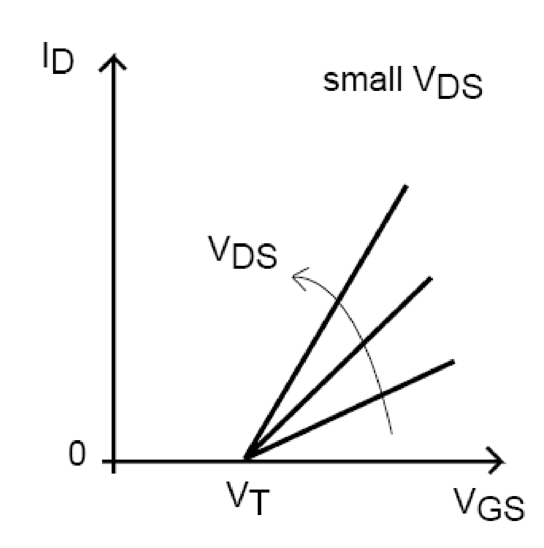
$V_{DS}\uparrow \rightarrow I_D\uparrow$ (higher lateral electric field)

$V_{GS}\uparrow \rightarrow I_D\uparrow$ (higher electron concentration)

$L\uparrow \rightarrow I_D\downarrow$ (lower lateral electric field)

$W\uparrow \rightarrow I_D\uparrow$ (wider conduction channel)





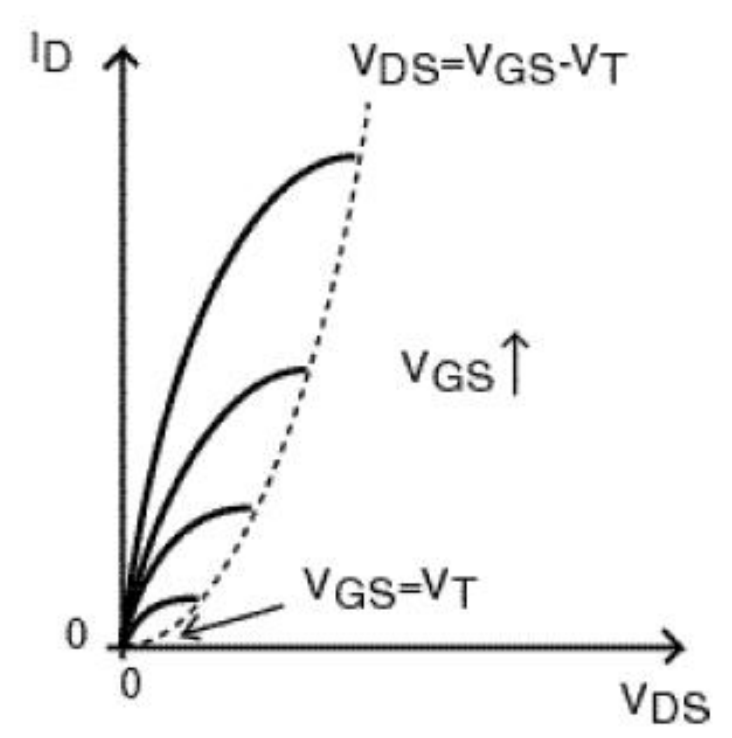
This is the *linear* or *triode* region:

It is linear if $V_{DS} << V_{GS} - V_T$

Two important observations

1. Equation only valid if $V_{GS} - V(y) \geq V_T$ at every y. Worst point is $y=L$, where $V(y) = V_{DS}$, hence, equation is valid if

$$V_{DS} \leq V_{GS} - V_T$$

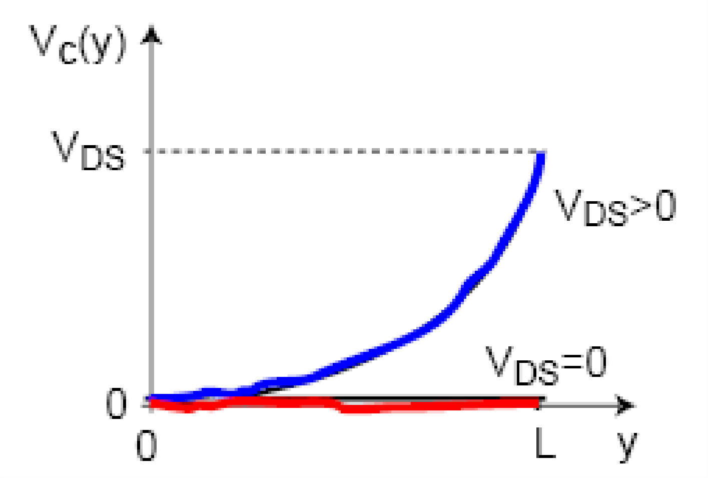


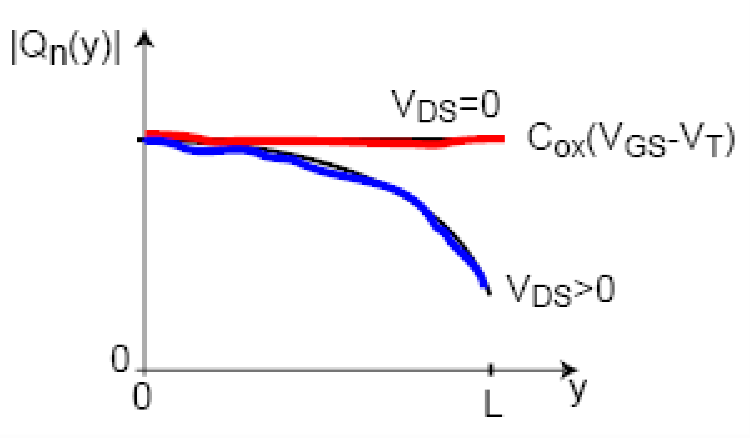
2. As V_{DS} approaches $V_{GS} - V_T$, the rate of increase of I_D decreases.

To understand why I_D bends over, must understand first : channel ***debiasing!***

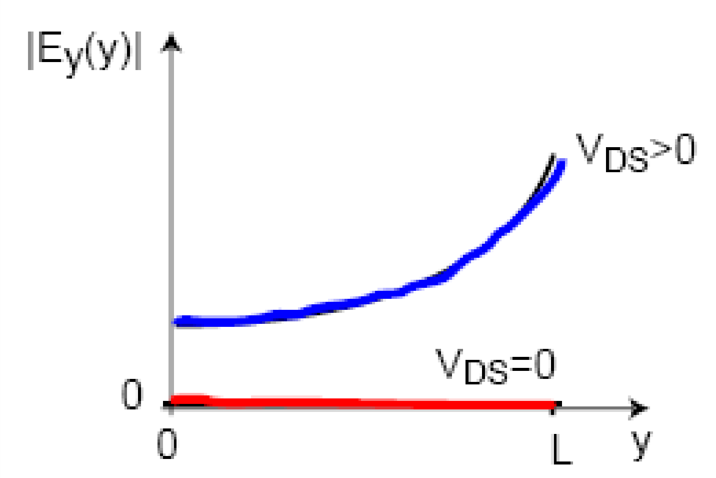
As y increases down the channel, $V(y)$ ↑, $|Q_N(y)|$ ↓, and $E_y(y)$ ↑ **(fewer carriers moving faster)**

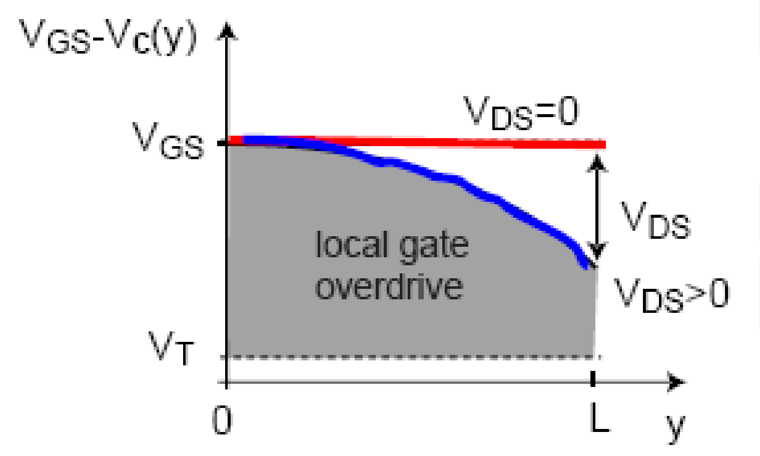
⇒inversion layer thins down from source to drain
⇒Local ”channel overdrive” reduced closer to drain.
⇒I_D grows more slowly.



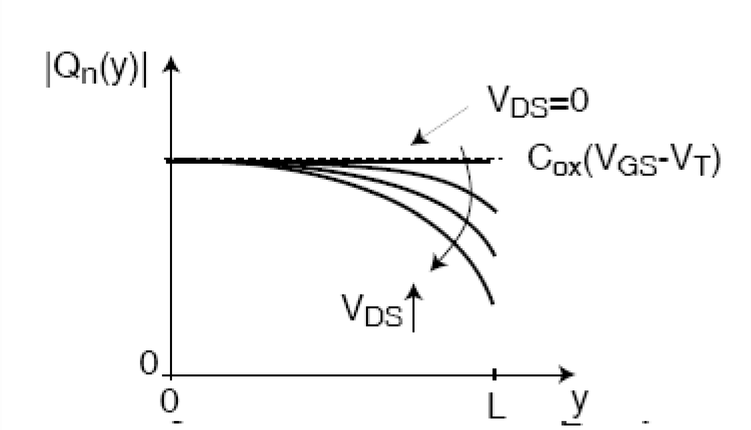


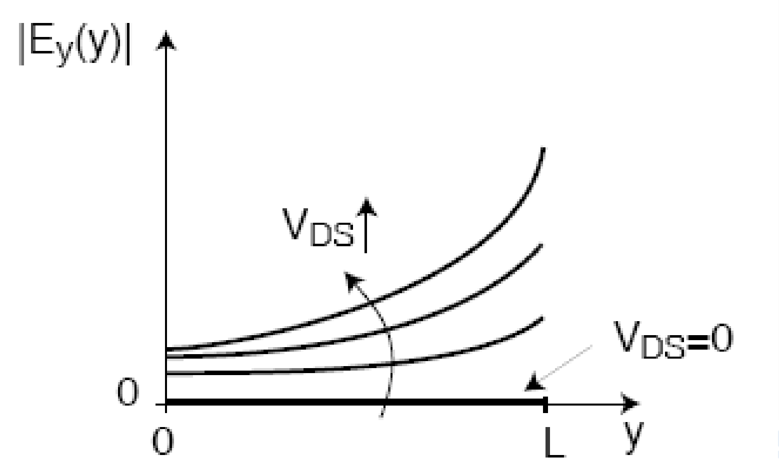
$$Q_N(y) = -C_{ox}\left[V_{GS} - V(y) - V_T\right]$$

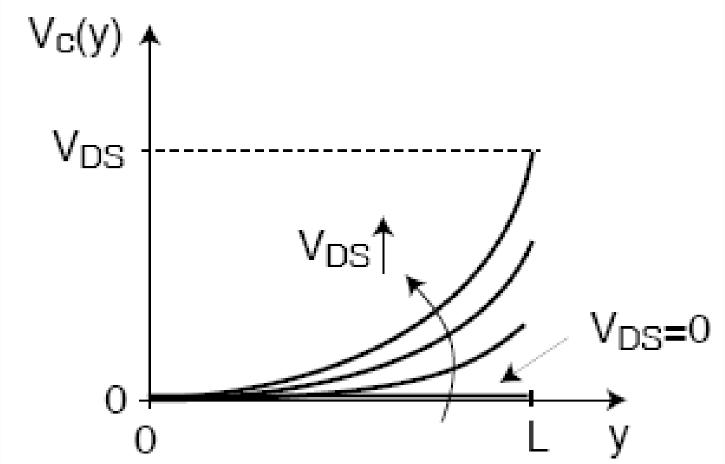


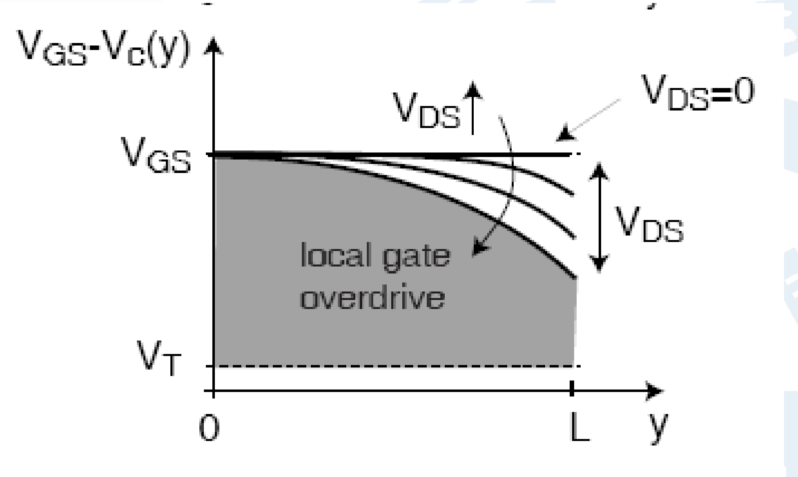


Impact of V_{DS}:









As V_{DS} ↑, channel debiasing more prominent
=> I_D rises more slowly with V_{DS}

Key conclusions

- The MOSFET is a field-effect transistor:
  - the amount of charge in the inversion layer is controlled by the field-effect action of the gate
  - the charge in the inversion layer is mobile ⇒ conduction possible between source and drain
- In the linear regime:
  - $V_{GS}\uparrow \Rightarrow I_D\uparrow$: more electrons in the channel
  - $V_{DS}\uparrow \Rightarrow I_D\uparrow$: stronger field pulling electrons out of the source
- Channel debiasing: inversion layer ”thins down” from source to drain ⇒ current saturation as V_{DS} approaches:

$$V_{DSsat}=V_{GS}-V_T$$

Drain current saturation

As V_{DS} approaches

$$V_{DSsat} = V_{GS} - V_T$$

increase in E_y compensated by decrease in $|Q_N|$
$\Rightarrow I_D$ saturates when $|Q_N|$ equals 0 at drain end.

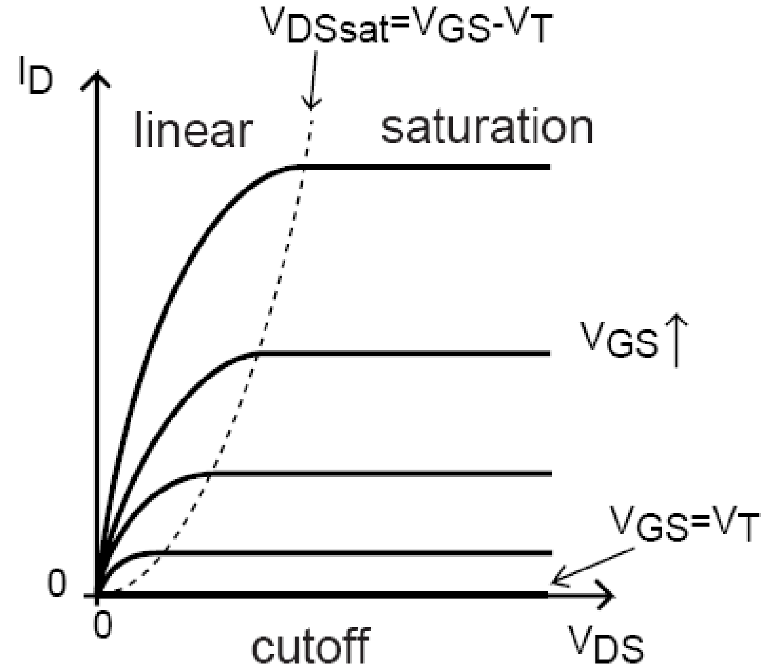
Value of drain saturation current:

$$I_{Dsat} = I_{Dlin}\left(V_{DS} = V_{DSsat} = V_{GS} - V_T\right)$$

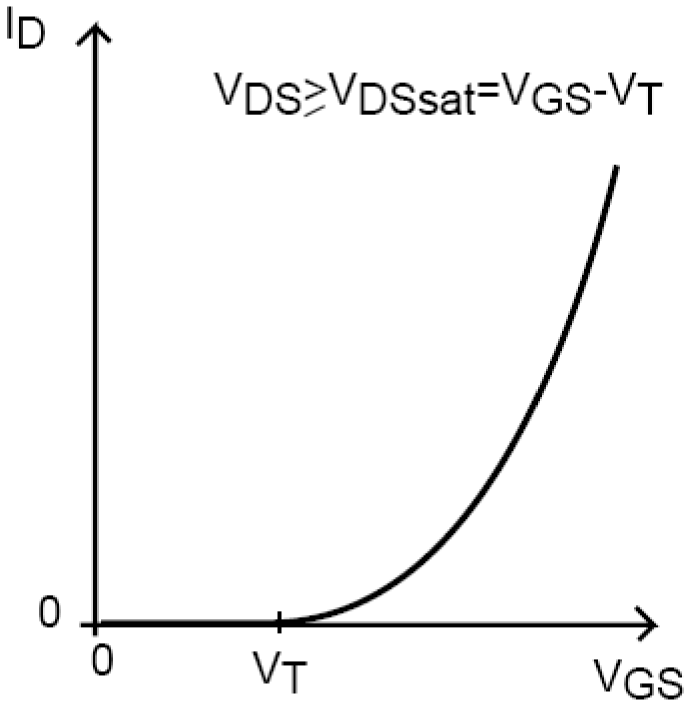
$$I_{Dsat} = \left[\frac{W}{L} \bullet \mu_n C_{ox}\left(V_{GS} - \frac{V_{DS}}{2} - V_T\right) \bullet V_{DS}\right]_{V_{DS}=V_{GS}-V_T}$$

$$\boxed{I_{Dsat} = \frac{1}{2}\frac{W}{L}\mu_n C_{ox}\left[\left(V_{GS} - V_T\right)\right]^2}$$

Output Characteristics



Transfer characteristics in saturation

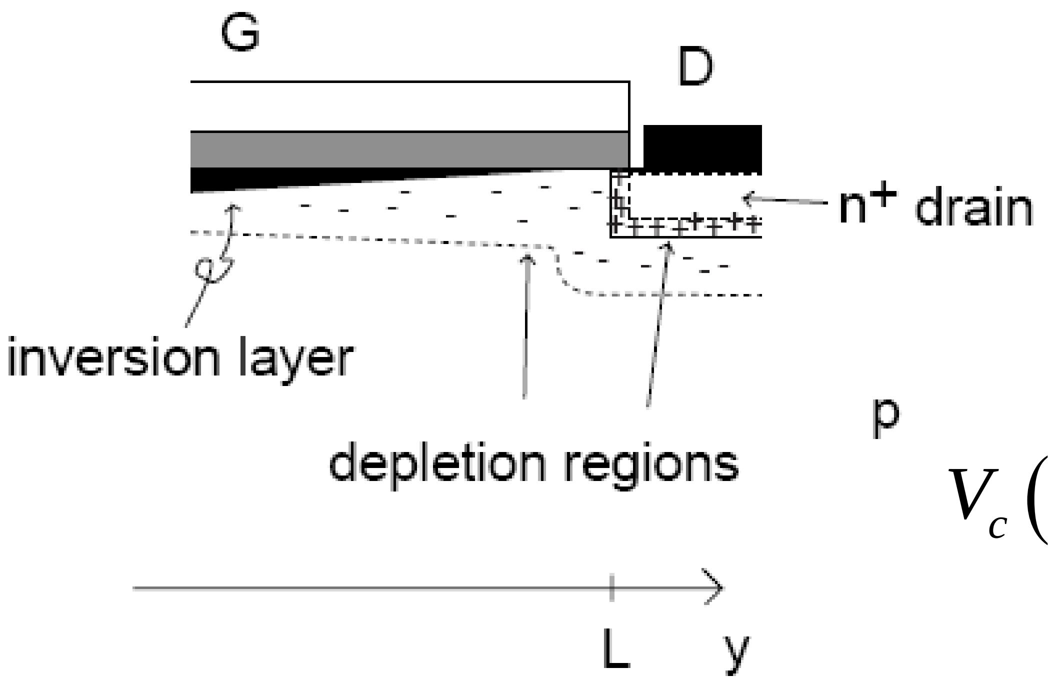


What happens when $V_{DS} = V_{GS} - V_T$?

Charge control relation at drain end of channel:

$$Q_n(L) = -C_{ox}\left(V_{GS} - V_{DS} - V_T\right) = 0$$

No inversion layer at end of channel??!! ⇒ Pinchoff



$$V_c(L) = V_{DSsat} = V_{GS} - V_T$$

Key dependencies of I_{Dsat}

$$I_{Dsat} \propto \left(V_{GS} - V_T\right)^2$$

Drain current at pinchoff:

$\propto$ lateral electric field $\propto V_{DSsat} = V_{GS} - V_T$

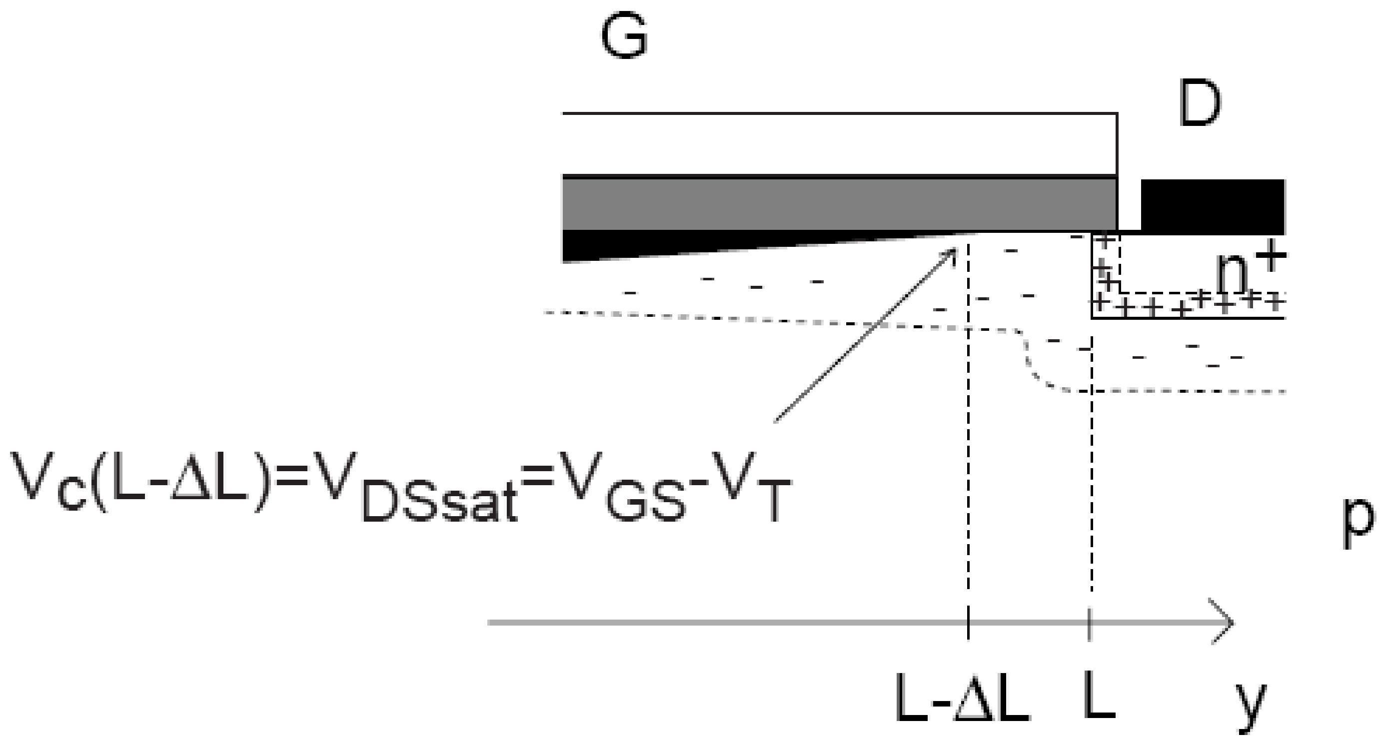
$\propto$ electron concentration $\propto V_{GS} - V_T$

$$I_{Dsat} \propto \frac{1}{L}$$

$$L \downarrow \rightarrow \left|E_y\right| \uparrow$$

What happens when $V_{DS} > V_{GS} - V_T$?

Depletion region separating pinchoff point and drain widens (just like in reverse biased pn junction)



To first order, I_D does not increase past pinchoff:

$$I_D = I_{Dsat} = \frac{W}{2L}\mu_n C_{ox}\left(V_{GS} - V_T\right)^2$$

To second order, electrical channel length affected (“channel length modulation”):

$$V_{DS}\uparrow \Rightarrow L_{channel}\downarrow \Rightarrow I_D\uparrow$$

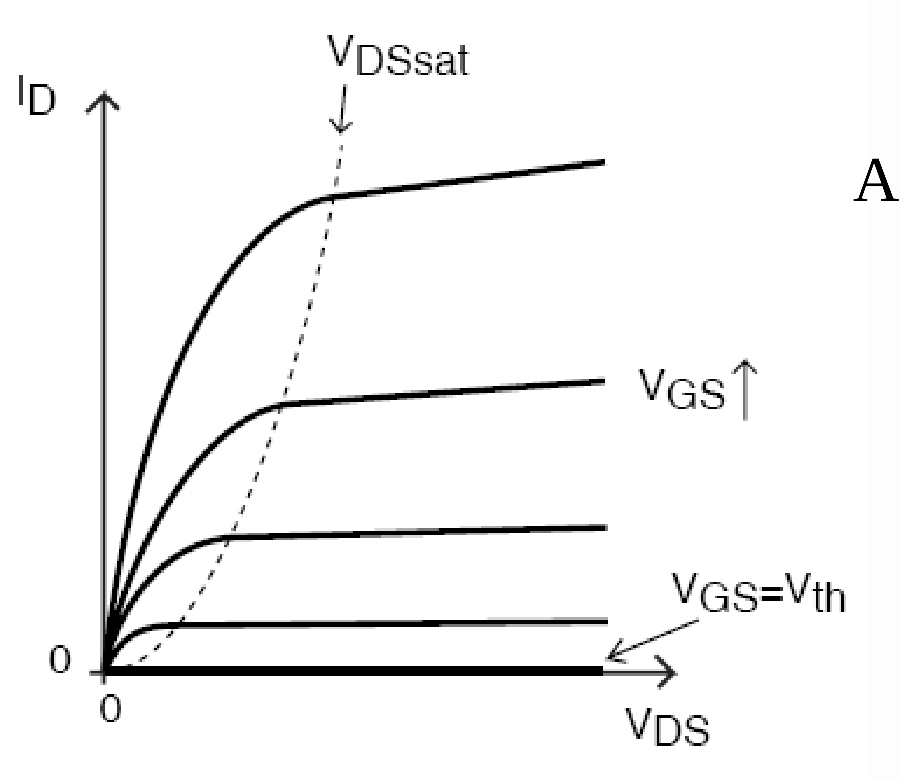
$$I_D \propto \frac{1}{L-\Delta L} \simeq \frac{1}{L}\left(1+\frac{\Delta L}{L}\right)$$

Experimental finding: $\Delta L \propto V_{DS} - V_{DSsat}$

Hence: $\dfrac{\Delta L}{L} = \lambda\left(V_{DS} - V_{Dsat}\right)$

Improved model in saturation:

$$I_{Dsat} = \frac{W}{2L}\mu_n C_{ox}\left(V_{GS} - V_T\right)^2\left[1 + \lambda\left(V_{DS} - V_{DSsat}\right)\right]$$



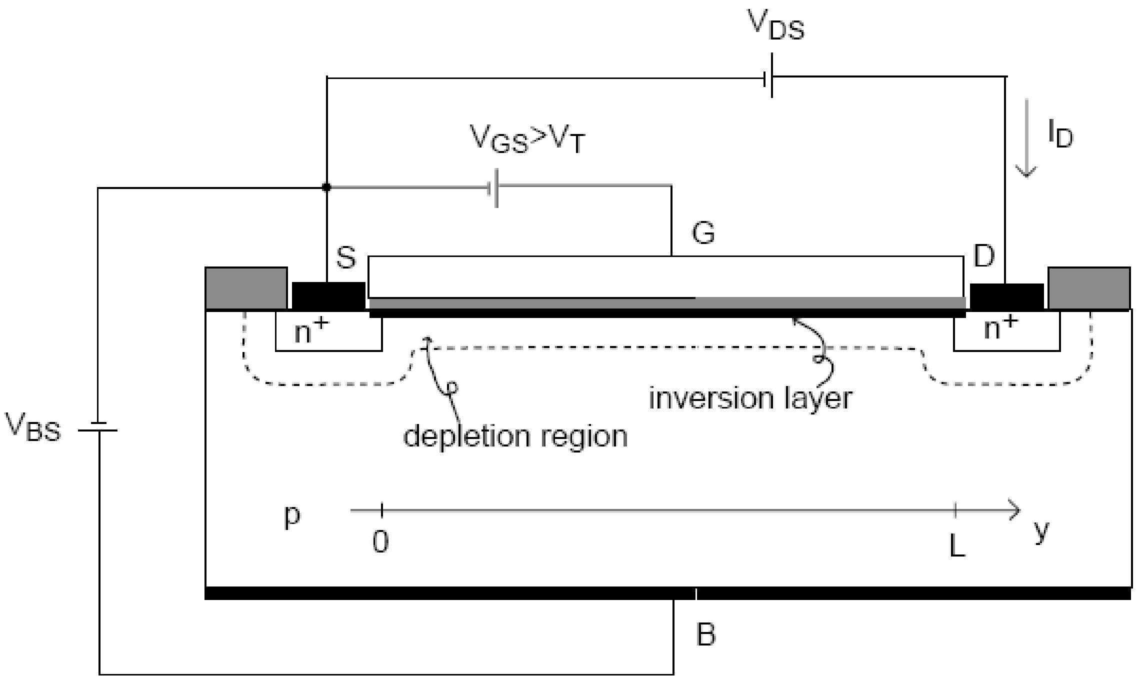
Also, experimental finding:

$$\lambda \propto \frac{1}{L}$$

2. Backgate characteristics

There is a fourth terminal in a MOSFET: the body.

What does the body do?



Body contact allows application of bias to body with respect to inversion layer, V_{BS}.

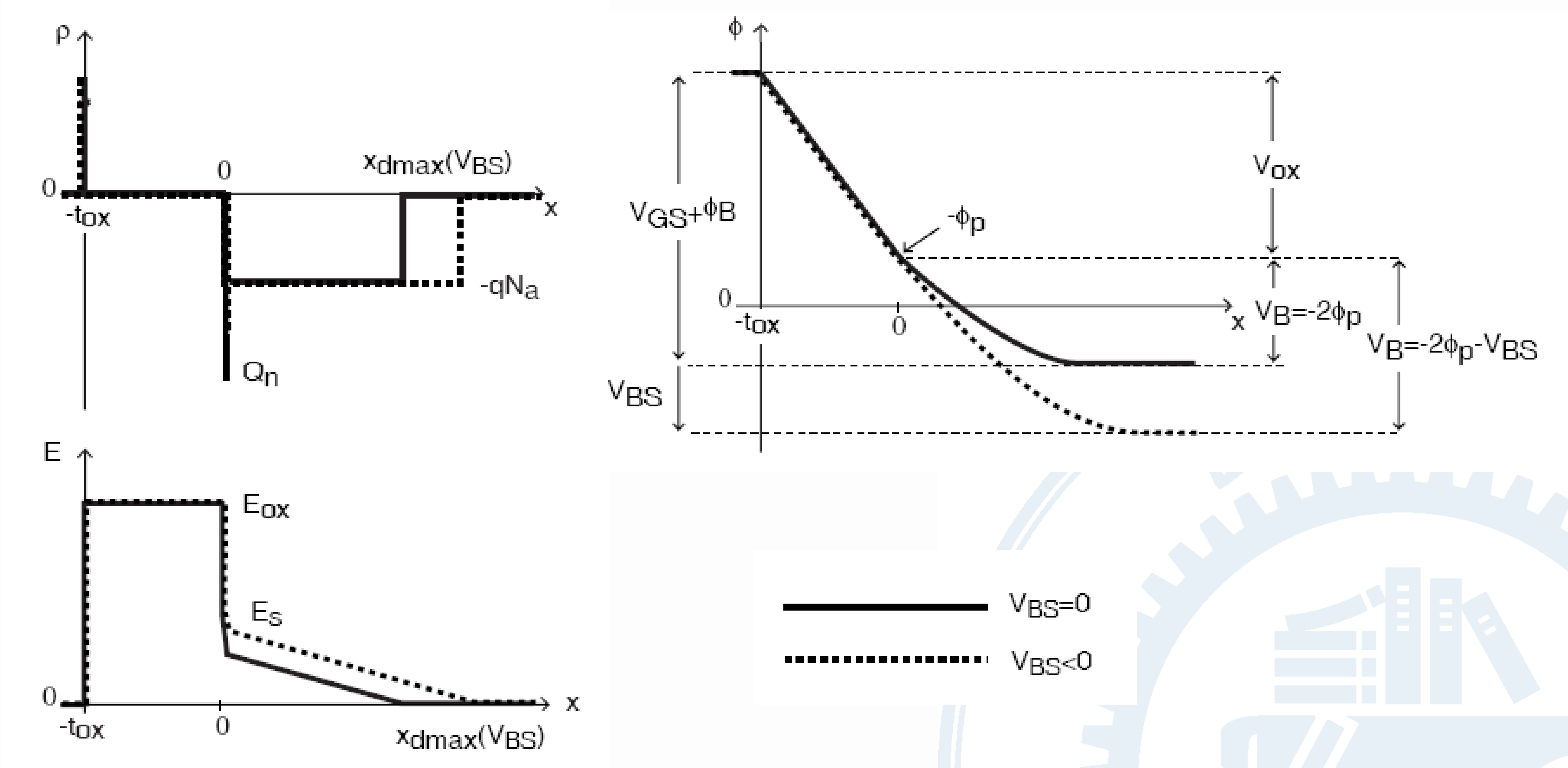
Only interested in $V_{BS}<0$ (pn diode in reverse bias).Interested in effect on inversion layer

$\Rightarrow$ examine for $V_{GS} > V_T$ (keep $\mathrm{V_{GS}}$ constant).

Application of $V_{BS} < 0$ increases potential buildup across semiconductor:

$$-2\phi_p \Rightarrow -2\phi_p - V_{BS}$$

Depletion region must widen to produce required extra field:


ρ
0
0
-tox
xdmax(VBS)
x
-qNa
Qn
E
Eox
Es
0
-tox
0
xdmax(VBS)
x
ϕ
VGS+ϕB
Vox
-ϕp
0
-tox
0
x
VB=-2ϕp
VB=-2ϕp-VBS
VBS
VBS=0
VBS<0

Consequences of application of $V_{BS} < 0$:

- $-2\phi_p \Rightarrow -2\phi_p - V_{BS}$
- $|Q_B| \uparrow \Rightarrow x_{d\max} \uparrow$
- since V_{GS} constant, V_{ox} unchanged

  $\Rightarrow$ E_{ox} unchanged

  $\Rightarrow$ $|Q_S| = |Q_G|$ unchanged

- $|Q_S| = |Q_n| + |Q_B|$ unchanged, but $|Q_B| \uparrow \Rightarrow |Q_n| \downarrow$

  $\Rightarrow$ inversion layer charge is reduced!

Application of $V_{BS} < 0$ with constant V_{GS} reduces electron concentration in inversion layer $\Rightarrow V_T \uparrow$

How does V_T *change with* V_{BS}?

In V_T formula change $-2\varphi_p$ to $-2\varphi_p - V_{BS}$:

$$V_T^{GB}\left(V_{BS}\right) = V_{FB} - 2\phi_p - V_{BS} + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_a\left(-2\phi_p - V_{BS}\right)}$$

In MOSFETs, interested in V_T between gate and source:

$$V_{GB} = V_{GS} - V_{BS} \Rightarrow V_T^{GB} = V_T^{GS} - V_{BS}$$

Then: $V_T^{GS} = V_T^{GB} + V_{BS}$

And: $V_T^{GS}\left(V_{BS}\right) = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_a\left(-2\phi_p - V_{BS}\right)} \equiv V_T\left(V_{BS}\right)$

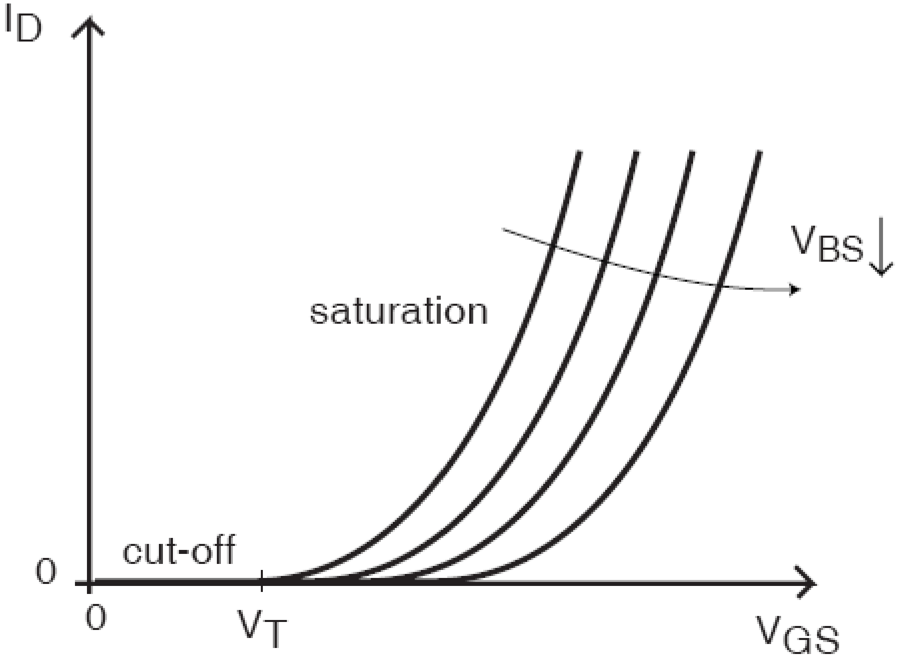
In the context of the MOSFET, V_T is always defined in terms of gate-to-source voltage.

Define **backgate effect parameter [units: *V*$^{1/2}$]:**

$$\gamma = \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_a}$$

Define $V_{To} = V_T\left(V_{BS} = 0\right)$ Zero-bias threshold voltage

Then : $V_T\left(V_{BS}\right) = V_{To} + \gamma\left(\sqrt{-2\phi_p - V_{BS}} - \sqrt{-2\phi_p}\right)$



Key conclusions

- *MOSFET in saturation ($V_{DS} \geq V_{DSsat}$):* pinchoff point at drain end of channel
  - – electron concentration small, but
  - – electrons move very fast;
  - – pinchoff point does not represent a barrier to electron flow
- In saturation, I_D saturates:

$$I_{Dsat} = \frac{W}{2L} \mu_n C_{ox} \left(V_{GS} - V_T\right)^2$$

•But due to channel length modulation, I_{Dsat} increases slightly with V_{DS}

•Application of back bias shifts V_T (backgate effect)

Example: MOSFET as a voltage controlled resistor

The circuit below shows an n-channel MOSFET that is used as voltage-controlled resistor.

(a) Find the sheet resistance of the MOSFET over the range V_{GS}=1.5 V to V_{GS}=4V using u_n= 215 cm^{2}V^{-1}S^{-1}, C_{ox}=2.3fF/um^2 and V_{tn} =1 V.

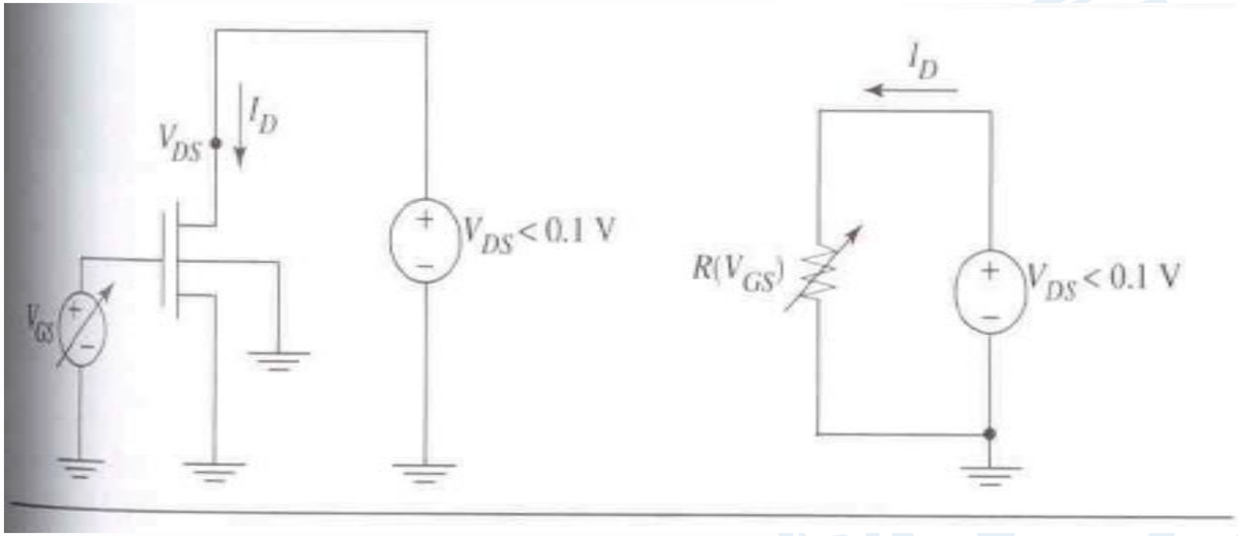


Fig. an n-channel MOSFET used a voltage controlled resistor

SOLUTION

Note that for a gate-source voltage $V_{GS} > V_{Tn} + 0.1V = 1.1V$, the MOSFET operates in the triode region. Since the drain-source voltage is small

$$I_D = \left(\frac{W}{L}\right)\mu_n C_{ox}\left(V_{GS} - V_{Tn}\right)V_{DS} = \frac{1}{R}V_{DS}$$

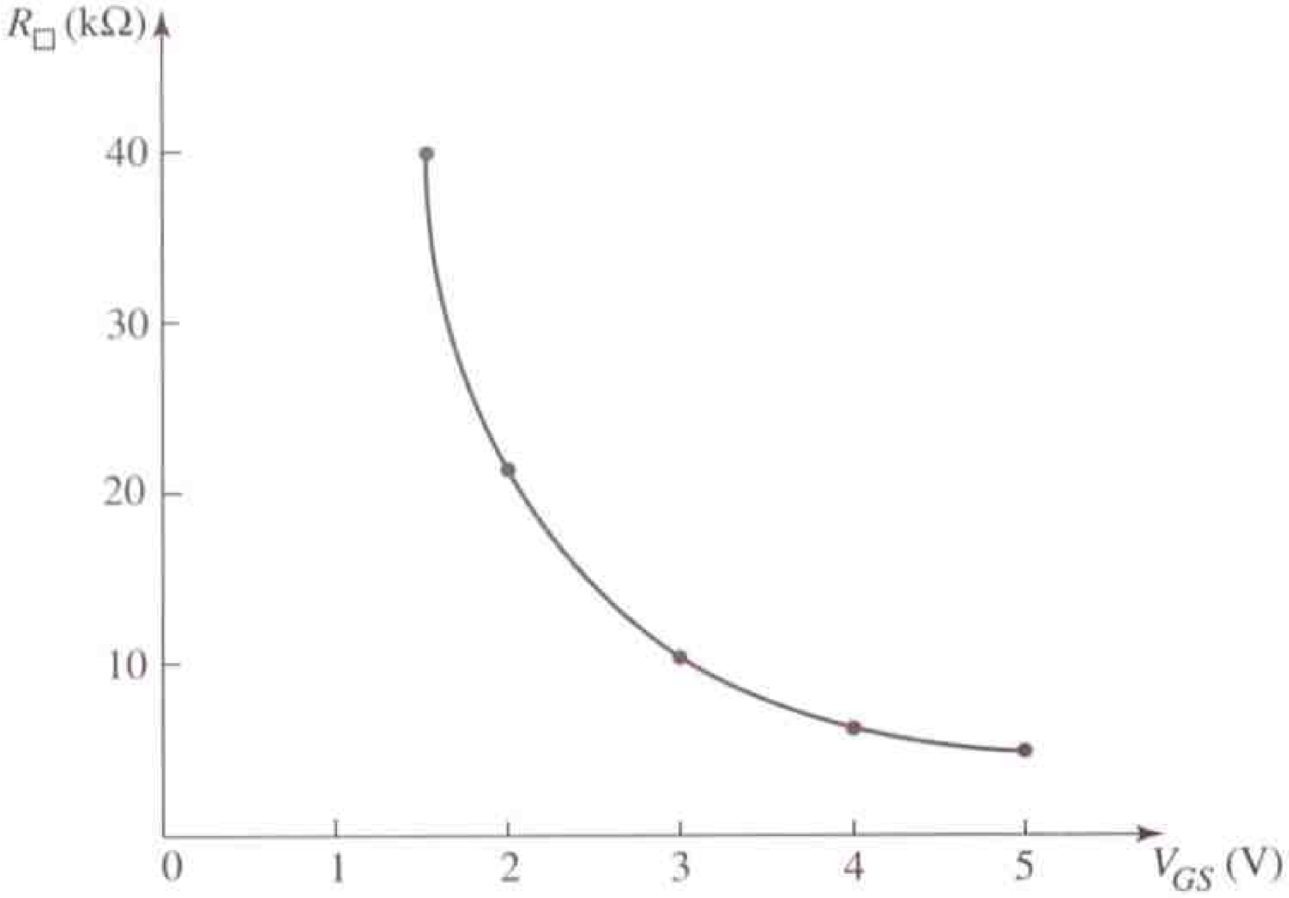
For a particular value of V_{GS}, I_D is a linear function of V_{DS} and the circuit model for the MOSFET is a resistor. Now we relate R to the sheet resistance

$$R = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS} - V_{Tn}\right)} = \frac{1}{\mu_n C_{ox}\left(V_{GS} - V_{Tn}\right)}\left(\frac{L}{W}\right) = R_{\square}\left(L/W\right)$$

$R_{\square}$ as a function of V_{GS} is

$$R_{\square} = \frac{1}{\left(215 cm^2 V^{-1} s^{-1}\right)\left(2.3 \times 10^{-7} F/cm^2\right)}\frac{1}{\left(V_{GS} - 1V\right)} = \frac{20k\Omega \cdot V}{V_{GS} - 1V}$$

The plot of sheet resistance as a function of V_{GS} with very small V_{DS}



(b) For a particular application, we need to control the resistor between 200 Ω and 1 kΩ for V_{GS}=1.5V to 4 V. How wide should the MOSFET be if the channel length L=1.5 um?

Solution:

We already solved for the sheet resistance in part (a), so we can find the range of sheet resistances for V_{GS}=1.5V to 4V

$$R_{\square\min} = \frac{20k\Omega\cdot V}{4V-1V} = 6666.7\Omega \text{ and } R_{\square\max} = \frac{20k\Omega\cdot V}{(1.5V-1V)} = 40k\Omega$$

Solving for (W/L) to obtain R_{min}=200 Ω and R_{max}=1 kΩ yields

$$\left(\frac{W}{L}\right)_{\min} = \frac{6666.7\Omega}{200\Omega} = 33.3 \text{ and } \left(\frac{W}{L}\right)_{\max} = \frac{40000\Omega}{1000\Omega} = 40$$

(W/L)=33.3 is adopted so the width of the MOSFET should be

$$W = 1.5\mu m(33.3) = 50\mu m$$

(c) Design the layout for this MOS resistor so it occupies a minimum area. The length of the source/drain diffusions is L_{diff}=6um with contact that are 2um × 2um.

Solution:
Given the high ratio of width to length (W/L=33.3), it is desirable to fold the MOSFET. Since the diffusions are 6 um long, the total length is

$$L_T = 3L_{diff} + 2L$$

$$= 3\times 6\text{um}+2\times 1.5\text{um}=21\text{um}$$

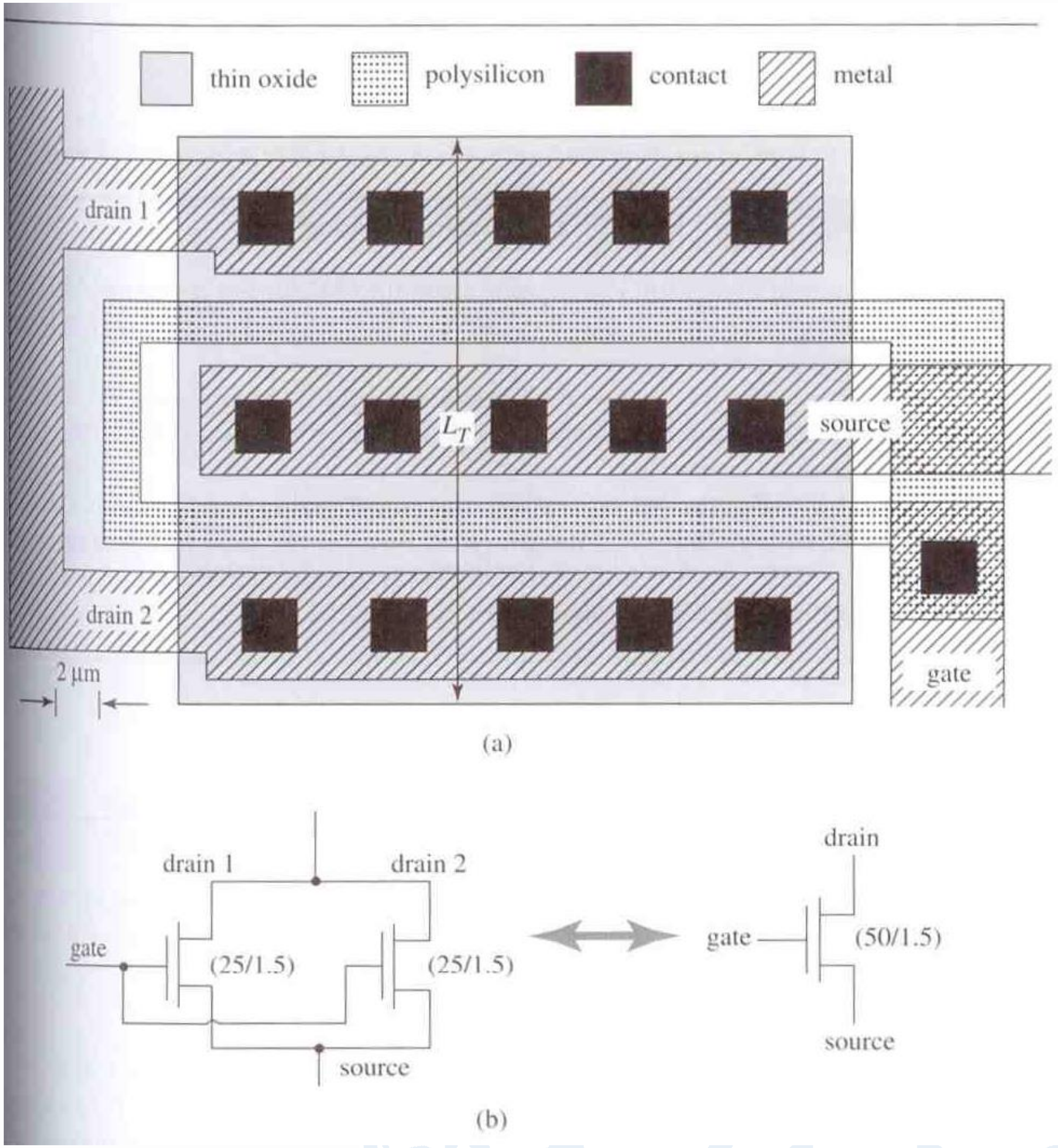


Fig (a) layout of folded n-channel MSOFET
(b) Equivalent schematic circuit

Example: Measuring the backgate effect parameter

The test circuit below can be used to find an experimental value for the backgate parameter γ_n. Note that a negative voltage V_{BS} is applied from the bulk to the source of the MOSFET. The circuit varies V_{GS} continuously from 0 to 5 V, for $V_{BS}=0$ $V_{BS}=-5V$. The drain-source voltage is $V_{DS}=100mV$.

(a) From the drain current measurements plotted below, find the backgate effect parameter. The device parameters are $u_n= 215$ cm^{2}V^{-1}S^{-1}, $C_{ox}=2.3$fF/um^2 , V_{t0} =1 V and $N_a=10^{17}$ cm^{-3}.

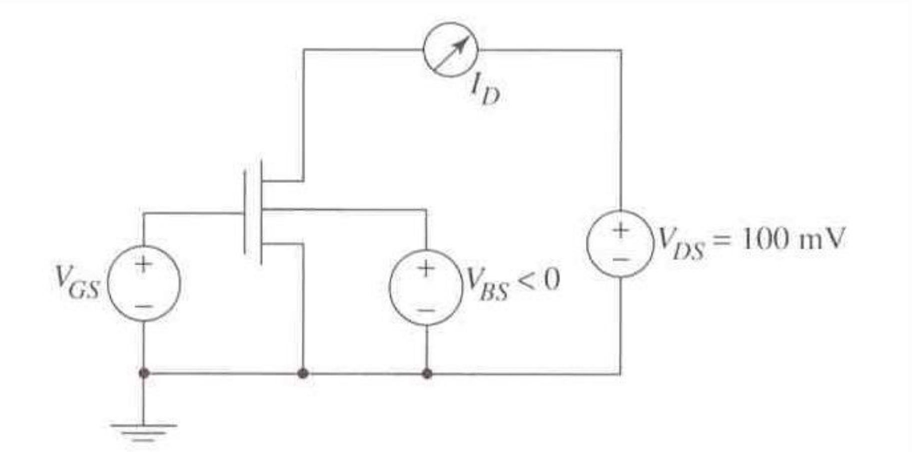
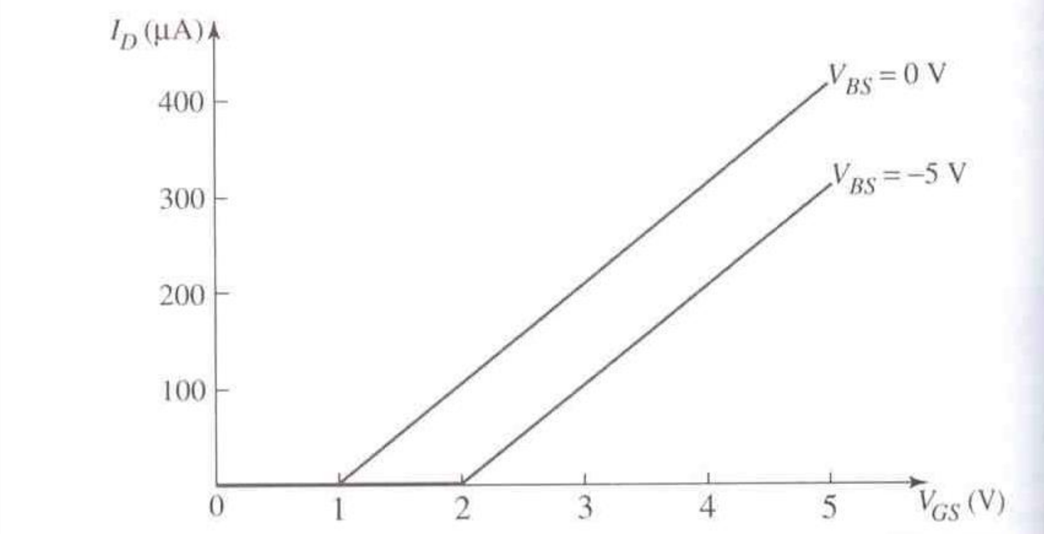


Fig. circuit to find the backgate effect parameter



Solution:

Since the drain voltage is small, the MOSFET operates in its triode region once V_{GS} exceeds the threshold voltage. The drain current is linear with V_{GS}

$$I_D \equiv \left(\frac{W}{L}\right)\mu_n C_{ox}\left[V_{GS} - V_{Tn}\left(V_{BS}\right)\right]V_{DS}$$

The threshold voltage is $V_T\left(V_{BS}\right) = V_{To} + \gamma\left(\sqrt{-2\phi_p - V_{BS}} - \sqrt{-2\phi_p}\right)$

From the graph, we have $2V = 1V + \gamma_n\left(\sqrt{\left(0.84V + 5V\right)} - \sqrt{0.84V}\right) \rightarrow \gamma_n = 0.67V^{1/2}$

Homework 15

Consider an n-channel MOSFET with the following parameters: u_n/C_{ox}=0.18 mA/V^2, W/L =8, and V_T =0.4 V. Determine the drain current I_D for

(a) V_{GS} =0.8 V, V_{DS} = 0.2 V;
(b) V_{GS} = 0.8 V, V_{DS} = 1.2 V;
(c) V_{GS} = 0.8 V, V_{DS} = 2.5 V;
(d) V_{GS} = 1.2 V, V_{DS} = 2.5 V.