上海交通大学
SHANGHAI JIAO TONG UNIVERSITY

Lecture 15

MOSFET Equivalent Circuit Models

Outline

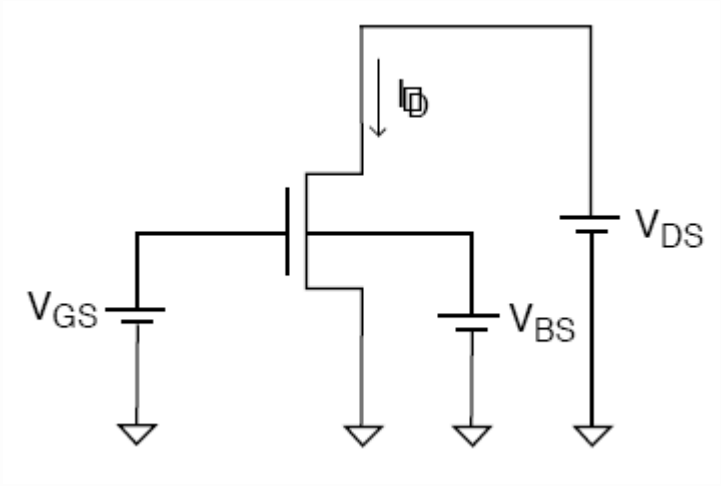
Large-signal model

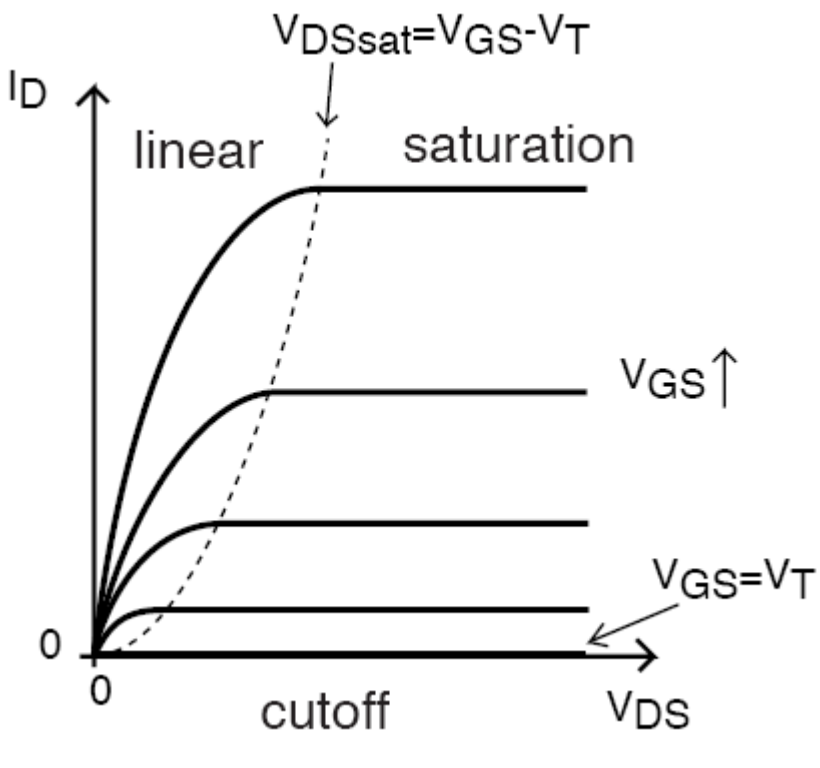
Low-frequency small-signal equivalent circuit model

High-frequency small-signal equivalent circuit model

Large Signal Model for NMOS Transistor

- **Regimes of operation:**





- **Cut-off**

$$I_D = 0$$

- **Linear / Triode:**

$$I_D = \frac{W}{L}\mu_n \left[V_{GS} - \frac{V_{DS}}{2} - V_T \right] \bullet V_{DS}$$

- **Saturation Regimes of operation:**

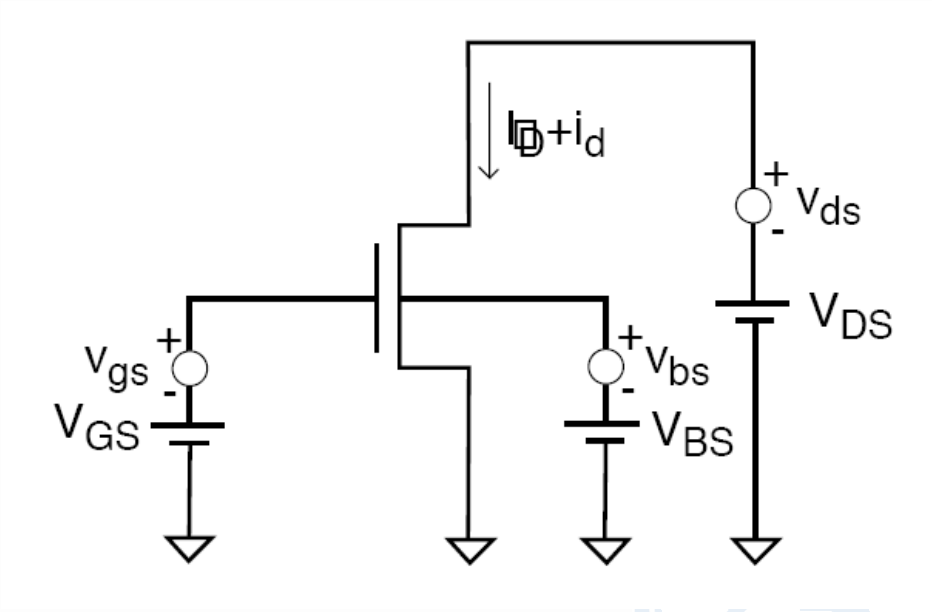
$$I_D = I_{Dsat} = \frac{W}{2L}\mu_n C_{ox} \left[V_{GS} - V_T \right]^2 \bullet \left[1 + \lambda V_{DS} \right]$$

- **Effect of back bias**

$$V_T\left(V_{BS}\right) = V_{To} + \gamma \left[\sqrt{-2\phi_p - V_{BS}} - \sqrt{-2\phi_P} \right]$$

Small-signal device modeling

In many applications, we are only interested in the response of the device to a small-signal applied on top of a bias.



Key Points:

- Small-signal is small
  – response of non-linear components becomes linear
- Since response is linear, lots of linear circuit techniques such as superposition can be used to determine the circuit response.
- Notation: $i_D = I_D + i_d$ ---Total = DC + Small Signal

Mathematically:

$$i_D\left(V_{GS}, V_{DS}, V_{BS}; v_{gs}, v_{ds}, v_{bs}\right) \approx$$
$$I_D\left(V_{GS}, V_{DS}, V_{BS}\right) + i_d\left(v_{gs}, v_{ds}, v_{bs}\right)$$

With i_d linear on small-signal drives:

$$i_d = g_m v_{gs} + g_0 v_{ds} + g_{mb} v_{bs}$$

Define g_m transconductance [S]

g_o output or drain conductance [S]

g_{mb} backgate transconductance [S]

Approach to computing g_m, g_o, and g_{mb}.

$$g_m \approx \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q \qquad Q = \left[v_{GS} = V_{GS}, v_{DS} = V_{DS}, v_{BS} = V_{BS}\right]$$

$$g_0 \approx \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q$$

$$g_{mb} \approx \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q$$

Transconductance

In saturation regime:

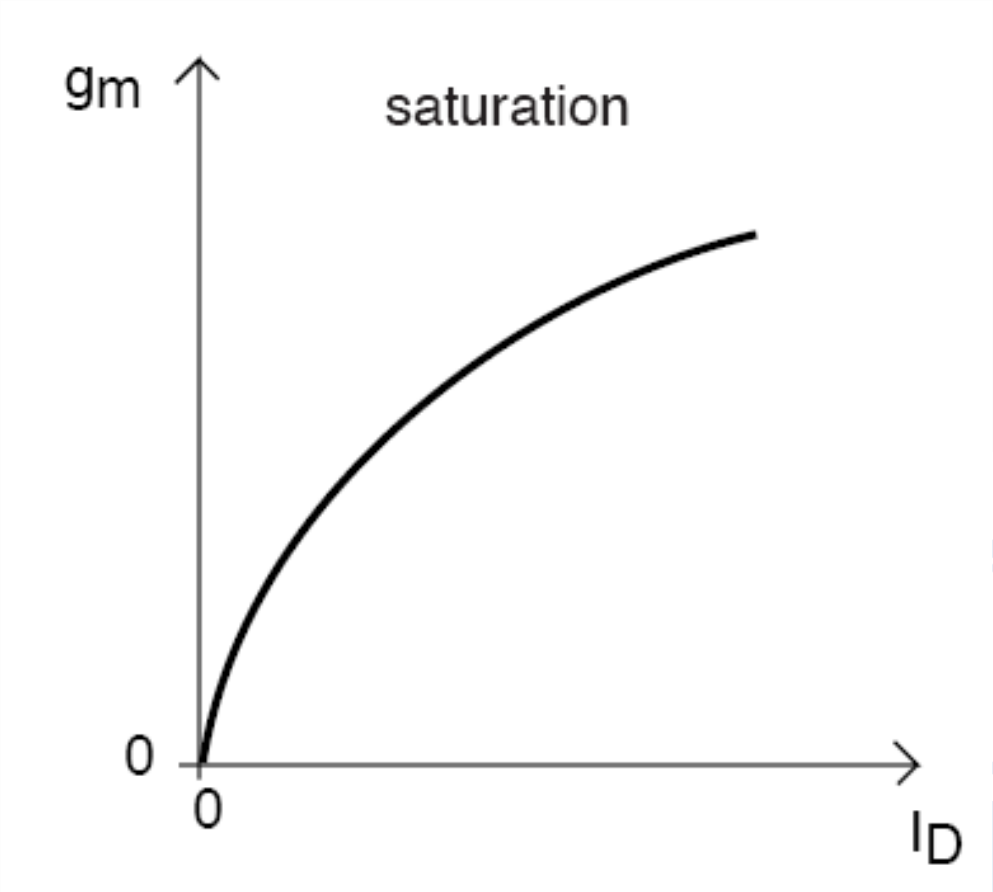
$$i_D = \frac{W}{2L}\mu_n C_{ox}\left[v_{GS} - V_T\right]^2 \bullet \left[1 + \lambda V_{DS}\right]$$

Then (neglecting channel length modulation) the transconductance is:

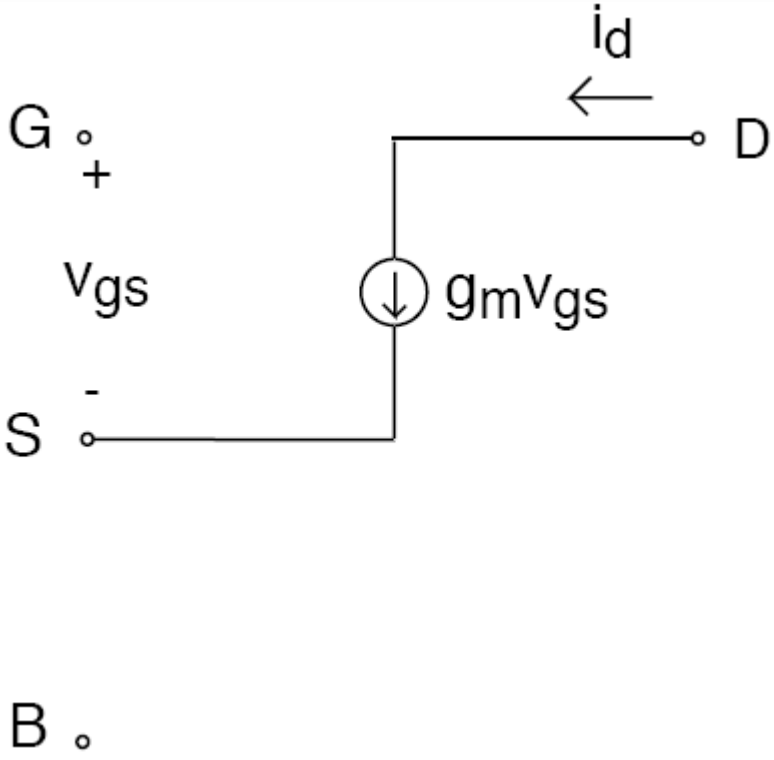
$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q \approx \frac{W}{L}\mu_n C_{ox}\left(V_{GS} - V_T\right)$$

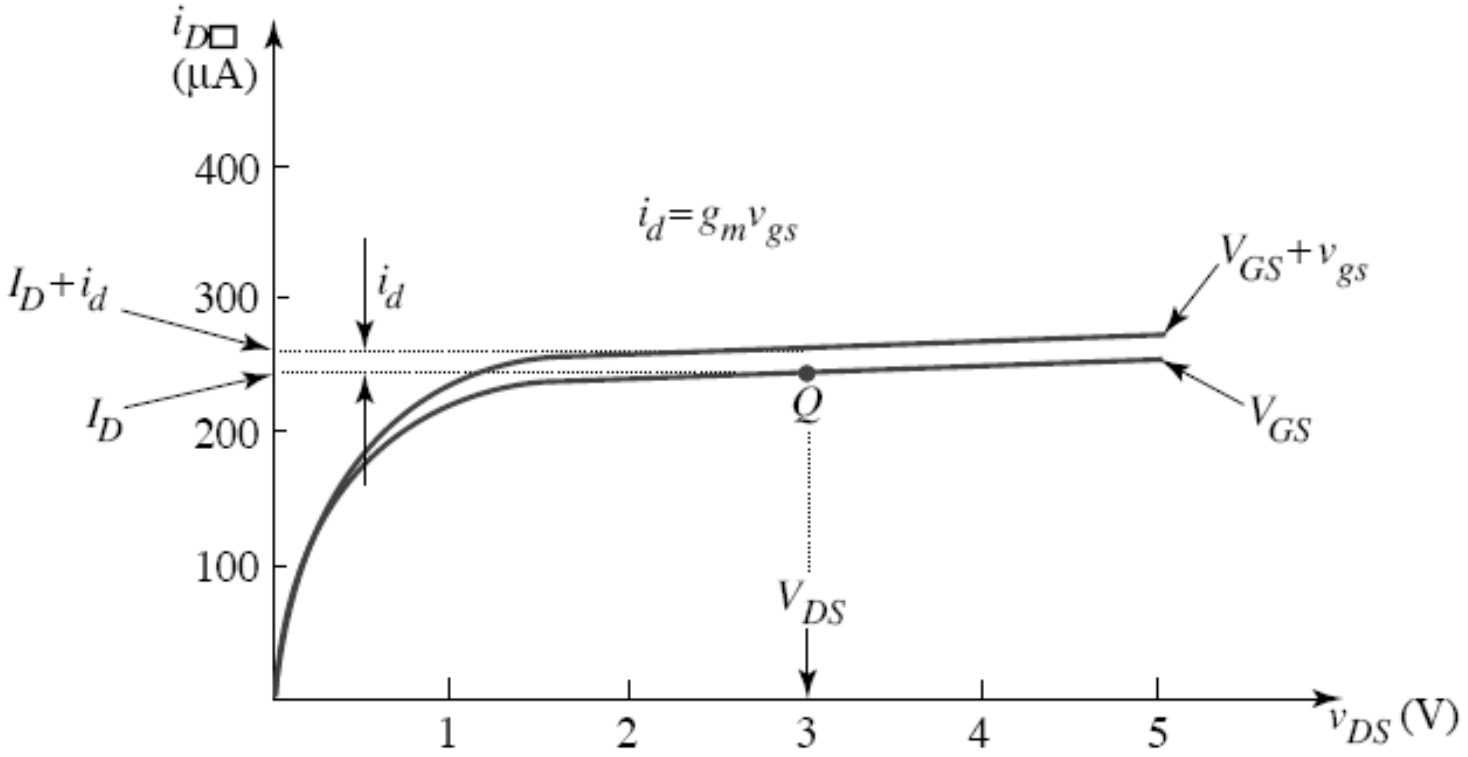
Rewrite in terms of I_D:

$$g_m = \sqrt{2\frac{W}{L}\mu_n C_{ox} I_D}$$


gm
saturation
0
0
I_D

Equivalent circuit model representation of g_m:




i_D (μA)
400
300
200
100
$I_D + i_d$
I_D
i_d
$i_d = g_m v_{gs}$
$V_{GS} + v_{gs}$
V_{GS}
Q
V_{DS}
1
2
3
4
5
v_{DS} (V)

Output conductance

In saturation regime:

$$i_D = \frac{W}{2L}\mu_n C_{ox}\left[v_{GS} - V_T\right]^2 \bullet \left[1 + \lambda v_{DS}\right]$$

Then:

$$g_0 = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q = \frac{W}{2L}\mu_n C_{ox}\left(V_{GS} - V_T\right)^2 \bullet \lambda \approx \lambda I_D$$

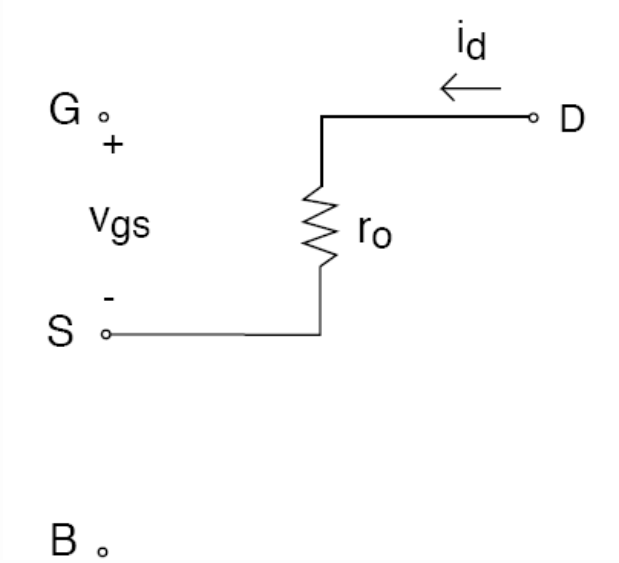
Output resistance is the inverse of output conductance:

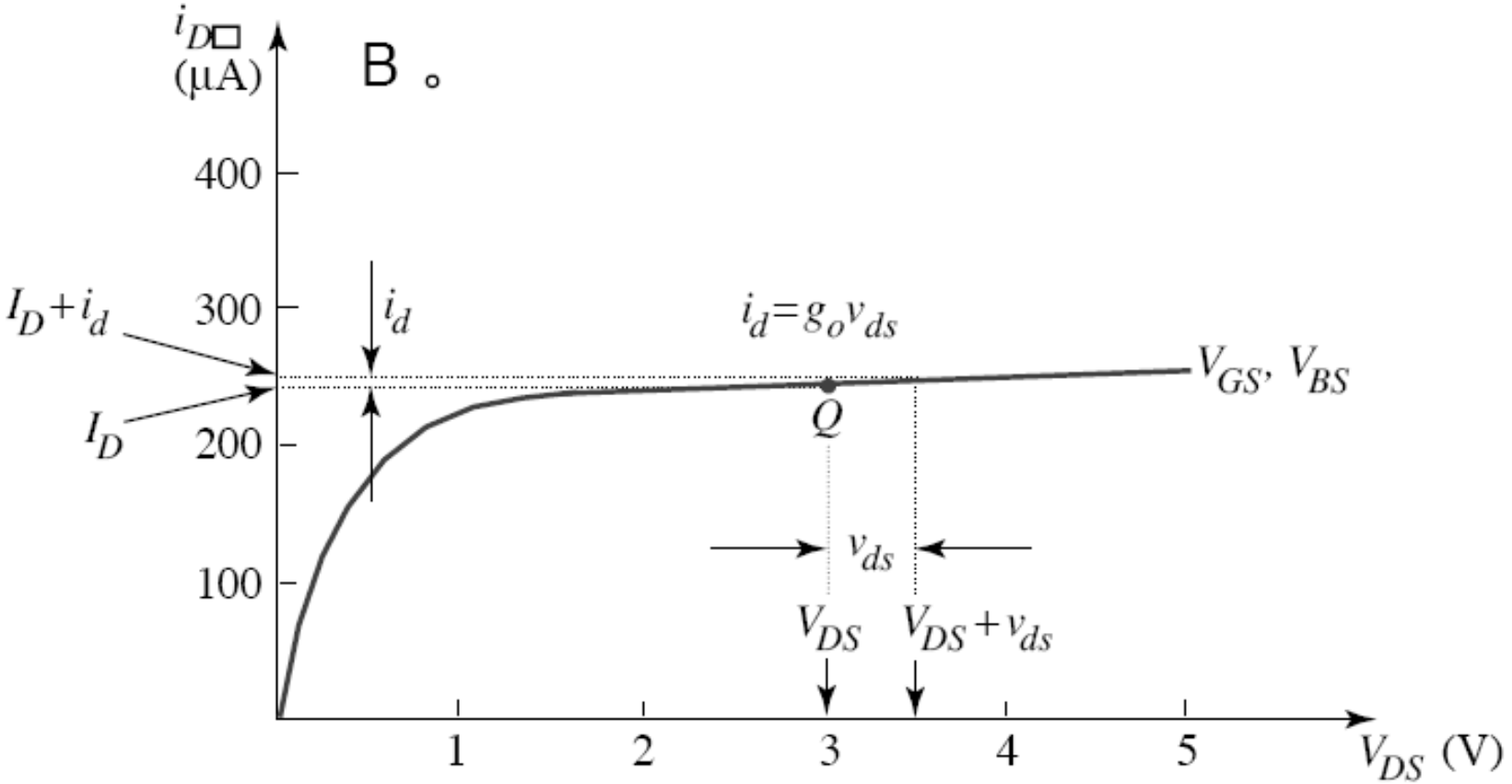
$$r_0 = \frac{1}{g_0} = \frac{1}{\lambda I_D}$$

Remember also: $\lambda \propto \frac{1}{L}$

Hence: $r_o \propto L$

Equivalent circuit model representation of g_o:




i_D□
(μA)
B 。
400
300
200
100
I_D+i_d
I_D
i_d
$i_d=g_o v_{ds}$
V_{GS}, V_{BS}
Q
v_{ds}
V_{DS}
$V_{DS}+v_{ds}$
1
2
3
4
5
V_{DS} (V)

Backgate transconductance

In saturation regime (neglect channel length modulation):

$$i_D \approx \frac{W}{2L}\mu_n C_{ox}\left[v_{GS} - V_T\right]^2$$

Then

$$g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q = -\frac{W}{L}\mu_n C_{ox}\left(V_{GS} - V_T\right)\bullet\left(\left.\frac{\partial V_T}{\partial v_{BS}}\right|_Q\right)$$

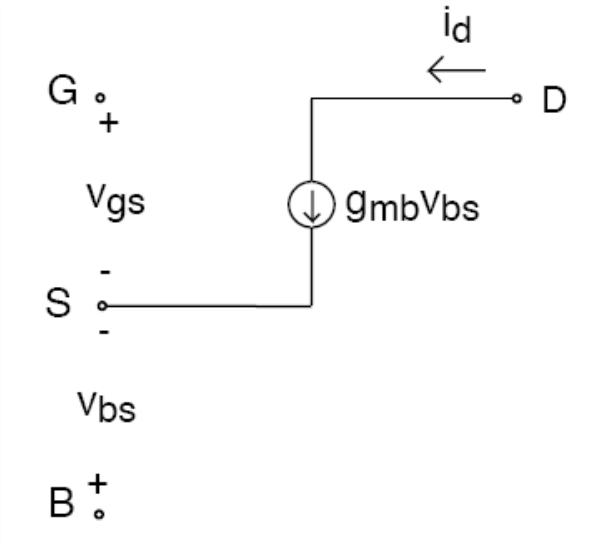
Since

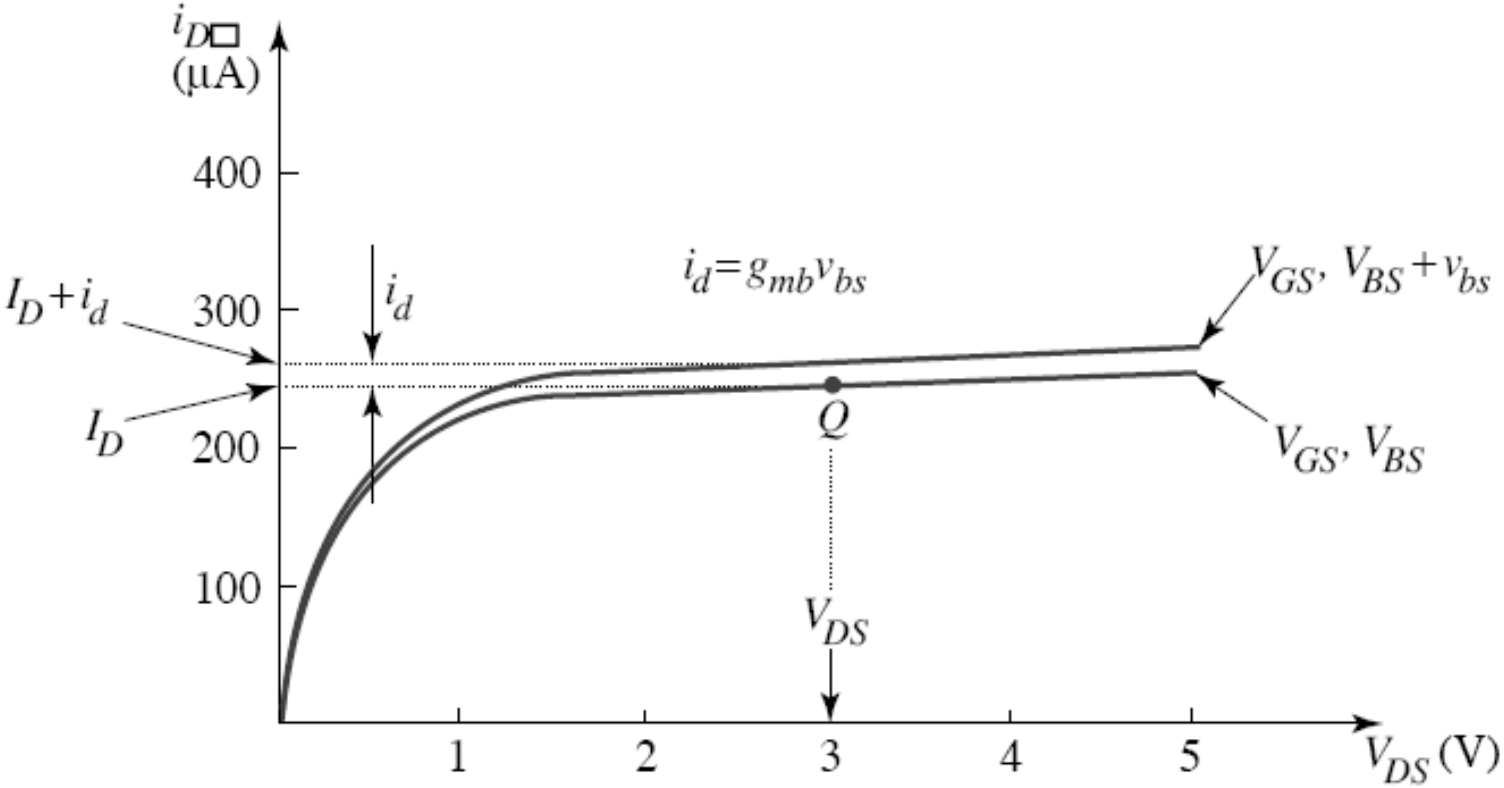
$$V_T\left(v_{BS}\right) = V_{T_0} + \gamma\left[\sqrt{-2\phi_p - v_{BS}} - \sqrt{-2\phi_p}\right]$$

$$\left.\frac{\partial V_T}{\partial v_{BS}}\right|_Q = \frac{-\gamma}{2\sqrt{-2\phi_p - V_{BS}}}$$

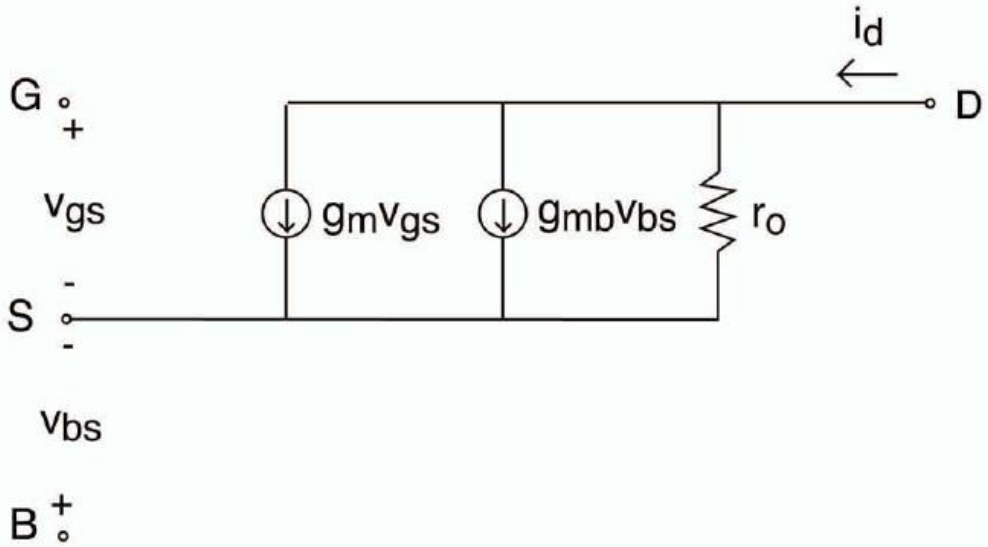
Hence: $$g_{mb} = \frac{\gamma g_m}{2\sqrt{-2\phi_p - V_{BS}}}$$

Equivalent circuit representation of g_{mb}:




i_D (μA)
400
300
200
100
$I_D + i_d$
I_D
i_d
$i_d = g_{mb} v_{bs}$
V_{GS}, $V_{BS} + v_{bs}$
V_{GS}, V_{BS}
Q
V_{DS}
1
2
3
4
5
V_{DS} (V)

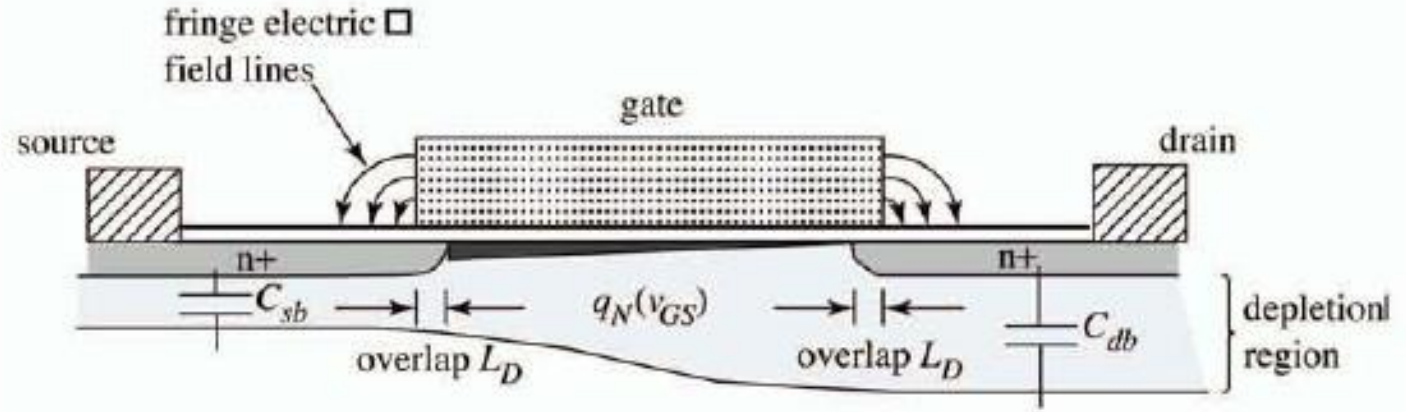
Complete MOSFET small-signal Equivalent circuit model for low frequency:



High-frequency small-signal equivalent circuit model

Need to add capacitances and resistance.

In saturation:



C_{gs} = channel charge + overlap capacitance C_{ov},
C_{gd}= overlap capacitance, C_{ov},
C_{Sb}= source junction depletion capacitance (+sidewall)
C_{db} = drain junction depletion capacitance (+sidewall)

ONLY Channel Charge Capacitance is intrinsic to device operation. All others are parasitic.

Inversion layer charge in saturation

$$q_N(v_{GS}) = W\int_0^L Q_N(y)\,dy = W\int_0^{v_{GS}-V_T} Q_N(v_C)\bullet\frac{dy}{dv_C}\bullet dv_C$$

Note that q_N is total inversion charge in the channel & $v_C(y)$ is the channel voltage. But:

$$\frac{dv_C}{dy} = -\frac{i_D}{W\mu_n Q_N(v_C)} \quad \Leftarrow$$

$$I_D = -W\bullet Q_N(y)\bullet v_y(y)$$

$$v_y(y) = -\mu_n\bullet E_y(y) = \mu_n\bullet\frac{dV}{dy}$$

Then:

$$q_N(v_{GS}) = -\frac{W^2\mu_n}{i_D}\bullet\int_0^{V_{GS}-V_T}\left[Q_N(v_C)\right]^2\bullet dv_C$$

Remember: $Q_N(v_C) = -C_{ox}\left[v_{GS} - v_C(y) - V_T\right]$

Then:

$$q_N(v_{GS}) = -\frac{W^2 \mu_n C^2_{ox}}{i_D} \bullet \int_0^{v_{GS}-V_T} \left[v_{GS} - v_C(y) - V_T\right]^2 \bullet dv_C$$

Do integral, substitute i_D in saturation and get:

$$q_N(v_{GS}) = -\frac{2}{3} WLC_{ox}(v_{GS} - V_T)$$

Gate charge: $q_G(v_{GS}) = -q_N(V_{GS}) - Q_{B,\max}$

Intrinsic gate-to-source capacitance:

$$C_{gs,i} = \frac{dq_G}{dv_{GS}} = \frac{2}{3} WLC_{ox}$$

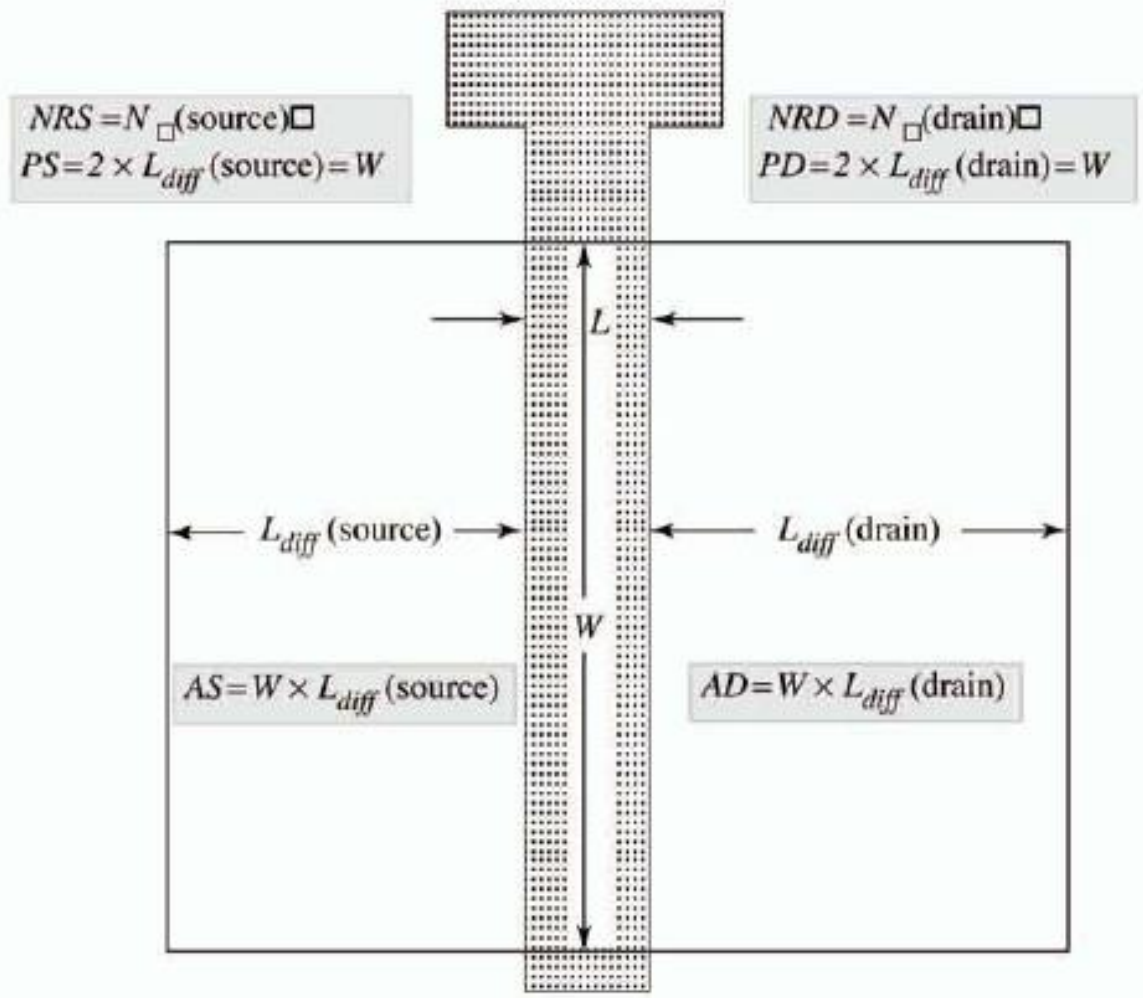
Must add overlap capacitance:

$$C_{gs} = \frac{2}{3}WLC_{ox} + WC_{ov}$$

Gate-to-drain capacitance — only overlap capacitance:

$$C_{gd} = WC_{ov}$$

Other capacitances



Source-to-Bulk capacitance:

$$C_{sb} = WL_{diff}C_j + (2L_{diff} + W)C_{jsw}$$

$$where \;\; C_j : Bottom\ Wall\ at\ V_{SB}(F/cm^2)$$

$$C_{jsw} : Side\ Wall\ at\ V_{SB}(F/cm)$$

Drain-to-Bulk capacitance:

$$C_{db} = WL_{diff}C_j + (2L_{diff} + W)C_{jsw}$$

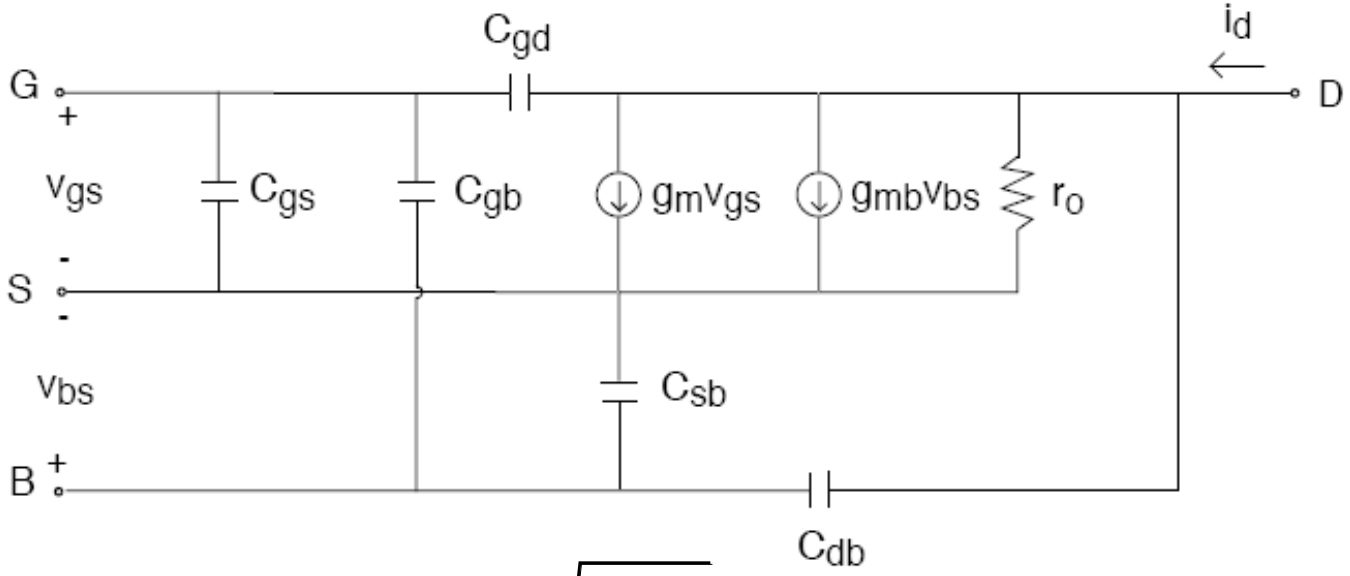
$$where \;\; C_j : Bottom\ Wall\ at\ V_{DB}(F/cm^2)$$

$$C_{jsw} : Side\ Wall\ at\ V_{DB}(F/cm)$$

Gate-to-Bulk capacitance:

$C_{gb} \equiv$ small parasitic capacitance in most cases (ignore)

High-frequency small-signal equivalent circuit model of MOSFET



$$g_m \propto \sqrt{\frac{W}{L} I_D}$$

In saturation:

$$r_0 \propto \frac{L}{I_D}$$

$$C_{gs} \propto WLC_{ox}$$

Frequency Limitation factors and Cutoff Frequency

Two frequency Limitation factors:

- Channel transit time
- Capacitance charging time – dominating factor

1. Channel transit time

$$\tau_t = \frac{L}{v}$$

The minimum channel transit time is

$$\tau_{t\min} = \frac{L}{v_{sat}}$$

The maximum frequency is

$$f_{\max} = \frac{1}{\tau_{t\min}}$$

2. Capacitance charging time

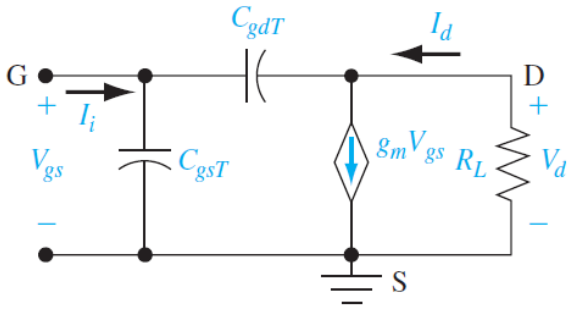


Fig. High frequency small signal model

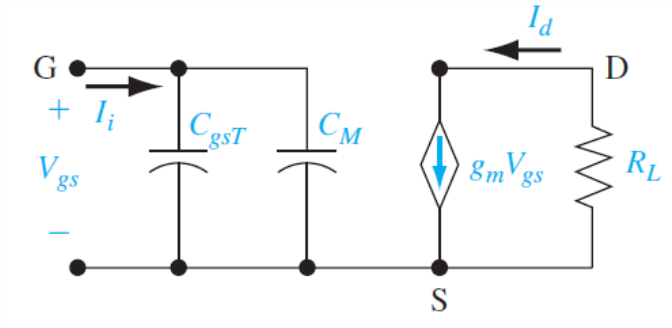


Fig. High frequency small signal equivalent circuit model including miller capacitance

The input current is

$$I_i = j\omega C_{gsT} V_{gs} + j\omega C_{gdT}(V_{gs} - V_d)$$

Summing the output current

$$\frac{V_d}{R_L} + g_m V_{gs} + j\omega C_{gdT}(V_d - V_{gs}) = 0$$

Combining the two equations to eliminate the voltage variable V_d , then

$$I_i = j\omega\left[C_{gsT} + C_{gdT}\left(\frac{1 + g_m R_L}{1 + j\omega R_L C_{gdT}}\right)\right]V_{gs}$$

Normally, $\omega R_L C_{gdT}$ is much less than unity

$$I_i = j\omega[C_{gsT} + C_{gdT}(1 + g_m R_L)]V_{gs}$$

The miller capacitance is then

$$C_M = C_{gdT}(1 + g_m R_L)$$

- **Cutoff frequency**

the frequency at which the magnitude of the current gain of the device is unity

$$I_i = j\omega(C_{gsT} + C_M)V_{gs} \qquad I_d = g_m V_{gs}$$

$$\left|\frac{I_d}{I_i}\right| = \frac{g_m}{2\pi f(C_{gsT} + C_M)} = 1$$

$$f_T = \frac{g_m}{2\pi(C_{gsT} + C_M)} = \frac{g_m}{2\pi C_G}$$

When the ideal MOSFET is biased in the saturation region, C_{gd} approaches zero and C_{gs} is approximately $C_{ox}WL$, and the transconductance is

$$g_{ms} = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_T)$$

The cutoff frequency is

$$f_T = \frac{g_m}{2\pi C_G} = \frac{\frac{W\mu_n C_{ox}(V_{GS} - V_T)}{L}}{2\pi C_{ox}WL} = \frac{\mu_n(V_{GS} - V_T)}{2\pi L^2}$$

- Source resistance effect

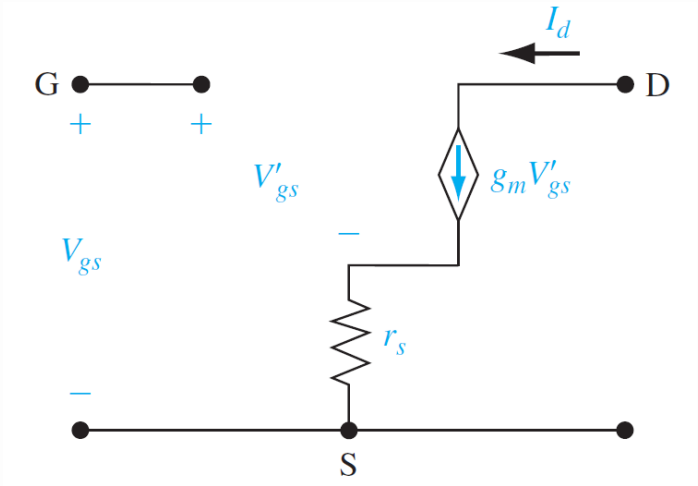


Figure Simplified, low frequency small-signal equivalent circuit of common-source n-channel MOSFET including source resistance

$$V_{gs} = V'_{gs} + (g_m V'_{gs}) r_s = (1 + g_m r_s) V'_{gs}$$

$$I_d = \left(\frac{g_m}{1 + g_m r_s} \right) V_{gs} = g'_m V_{gs}$$

The source resistance reduces the effective transconductance or transistor gain。

Homework16

Consider an ideal n-channel MOSFET with a width-to-length ratio of (W/L) =10, an electron mobility of un =400 cm^2 /V-s, an oxide thickness of t_{ox} =475 Å, and a threshold voltage of V_T =0.65 V.

(a) Determine the maximum value of source resistance so that the saturation transconductance g_{ms} is reduced by no more than 20 percent from its ideal value when V_{GS} =5 V.

(b) Using the value of r_s calculated in part (a), how much is g_{ms} reduced from its ideal value when V_{GS} =3 V?