Lecture 20

Transistor Amplifiers (II)

Contents:

- Common-drain amplifier
- Common-gate amplifier

Key questions

- What other amplifier stages can one build with a single MOSFET and a current source?
- What is the uniqueness of these other stages?

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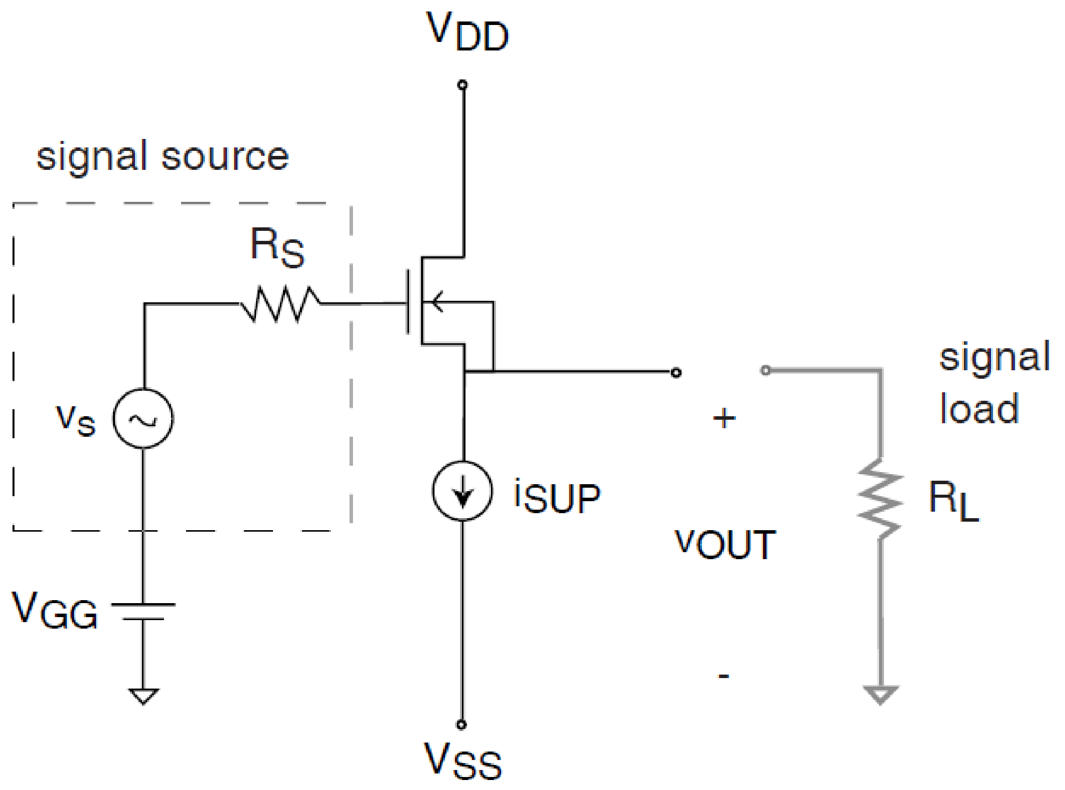
2. Common-drain amplifier

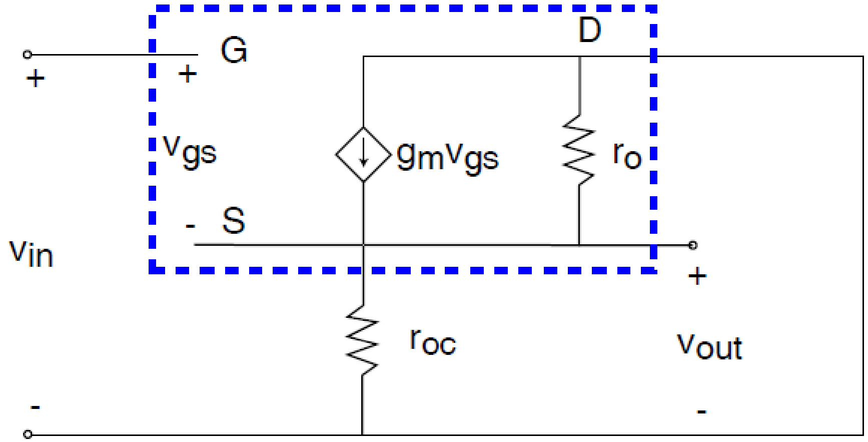


How does it work?

- V_{GG}, I_{SUP}, and *W/L* selected to bias MOSFET in saturation, obtain desired output bias point, and desired output swing.
- $v_{GG}\uparrow \Rightarrow i_D$ can't change $\Rightarrow v_{OUT}\uparrow$ (source follower)
- to first order, no voltage gain: $v_{out} \cong v_s$
- but R_{out} small: effective voltage buffer stage (good for making voltage amp in combination with common-source stage).

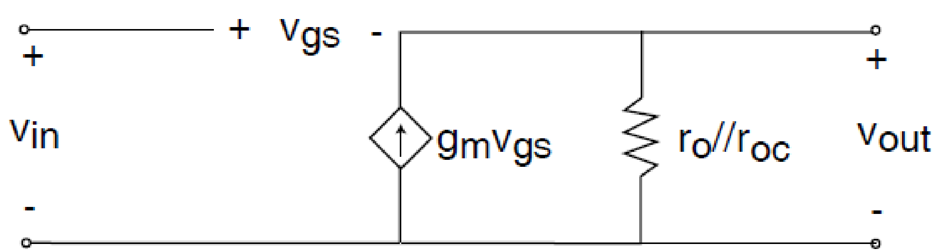
☐ Small-signal analysis

Unloaded small-signal equivalent circuit model:



$$v_{in} = v_{gs} + v_{out}$$

$$v_{out} = g_m v_{gs}(r_o // r_{oc})$$

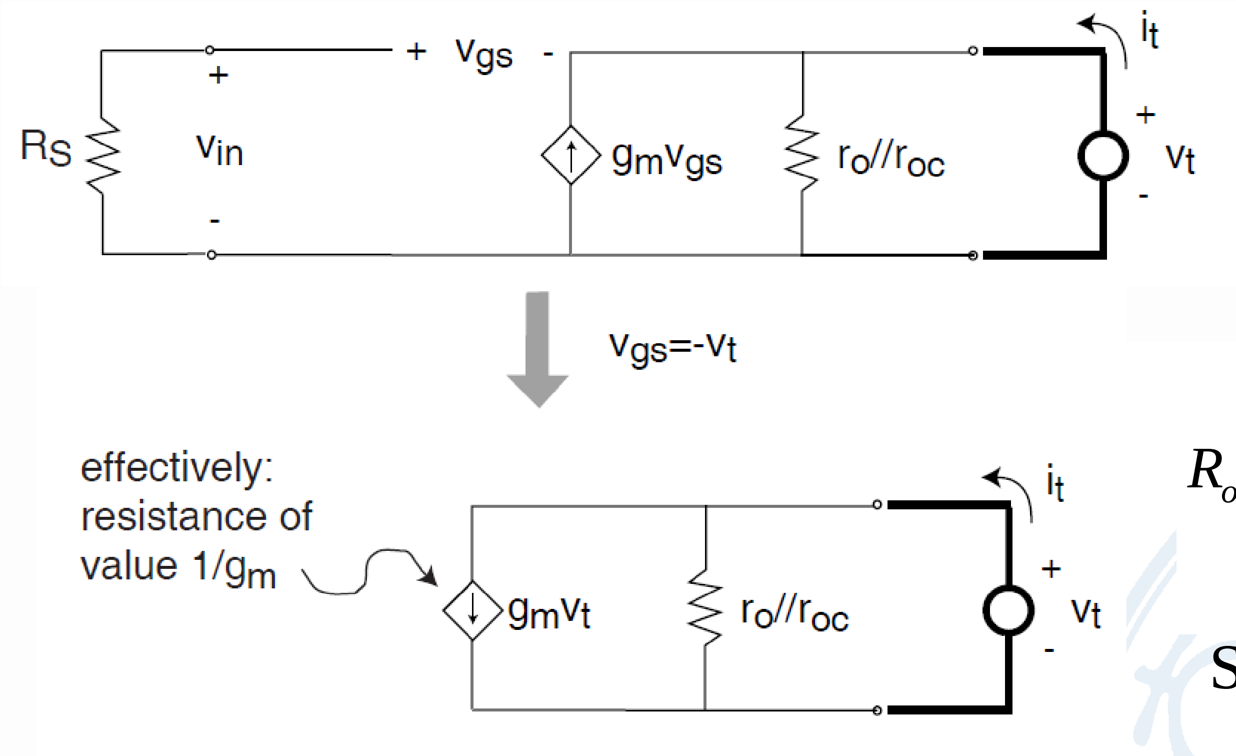


Then:

$$A_{vo} = \frac{g_m}{g_m + \frac{1}{r_O // r_{OC}}} \approx 1$$

Input impedance: $R_{in} = \infty$

Output impedance:



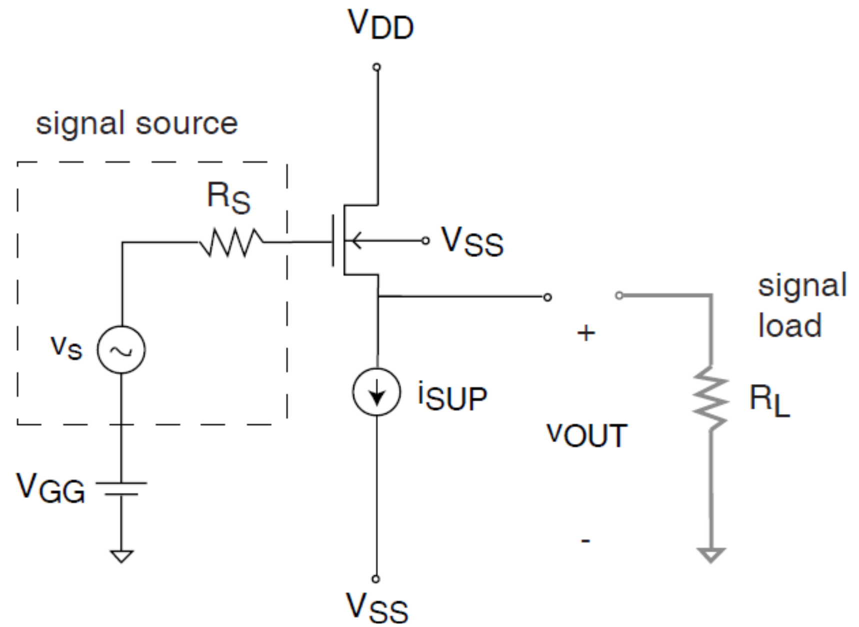
$$R_{out} = \frac{1}{g_m + \frac{1}{r_O // r_{OC}}} \approx \frac{1}{g_m}$$

Small!

Loaded voltage gain: $$A_v = A_{vo} \frac{R_L}{R_L + R_{out}} \approx \frac{R_L}{R_L + \frac{1}{g_m}} \approx 1$$

- Effect of back bias:

  If MOSFET not fabricated on isolated p-well, then body is tied up to wafer substrate (connected to V_{SS}):

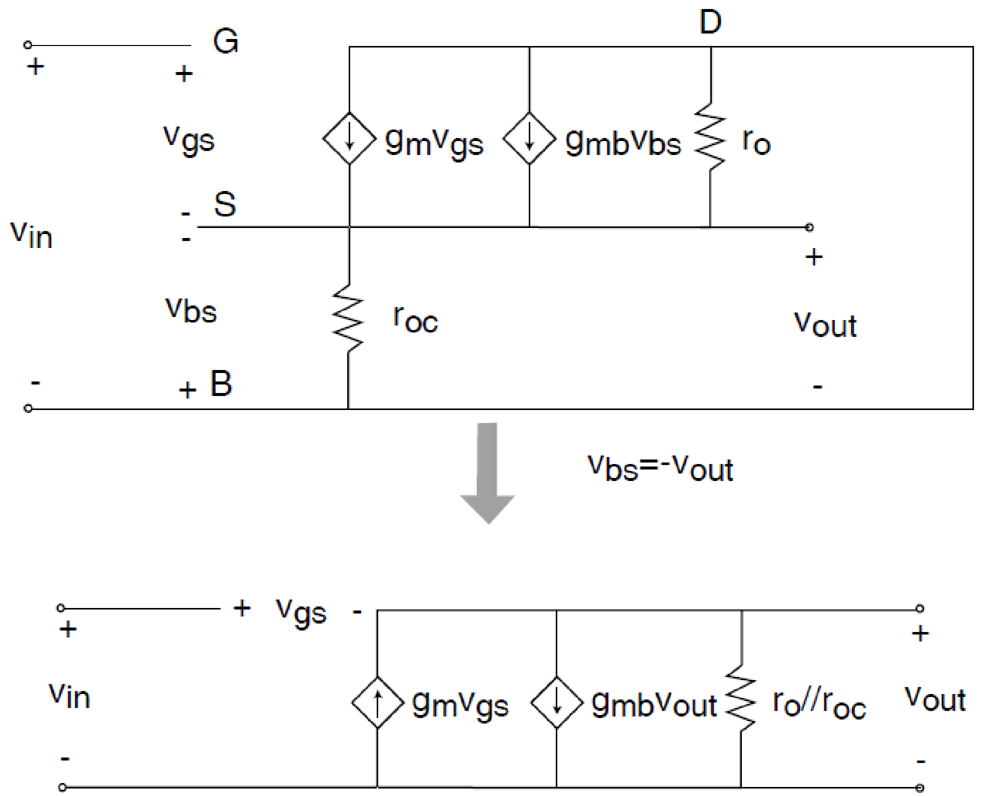


Two consequences:

Bias affected: V_T depends on $V_{BS} = V_{SS} - V_{OUT} \neq 0$

Small signal figures of merit affected: signal shows up between B and S ($v_{BS} = -v_{out}$).

Small signal equivalent circuit model:



$$A_{vo} = \frac{g_m}{g_m + g_{mb} + \frac{1}{r_O // r_{OC}}} \approx \frac{g_m}{g_m + g_{mb}} < 1 \qquad R_{out} = \frac{1}{g_m + g_{mb} + \frac{1}{r_O // r_{OC}}} \approx \frac{1}{g_m + g_{mb}}$$

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- Relationship between circuit figures of merit and device parameters:

$$g_m = \sqrt{2\frac{W}{L}\mu_n C_{ox} I_D} \qquad g_{mb} = \frac{\gamma}{2\sqrt{-2\phi_p - V_{BS}}} g_m$$

Device * Parameters	Circuit Parameters		
	$\lvert A_{vo} \rvert$	R_{in}	R_{out}
	$\frac{g_m}{g_m+g_{mb}}$	∞	$\frac{1}{g_m+g_{mb}}$
$I_{SUP} \uparrow$	-	-	$\downarrow$
$W \uparrow$	-	-	$\downarrow$
$\mu_n C_{ox} \uparrow$	-	-	$\downarrow$
$L \uparrow$	-	-	$\uparrow$

CD amp useful as a voltage buffer to drive small loads (in a multistage amp, other stages will be used to provide voltage gain).

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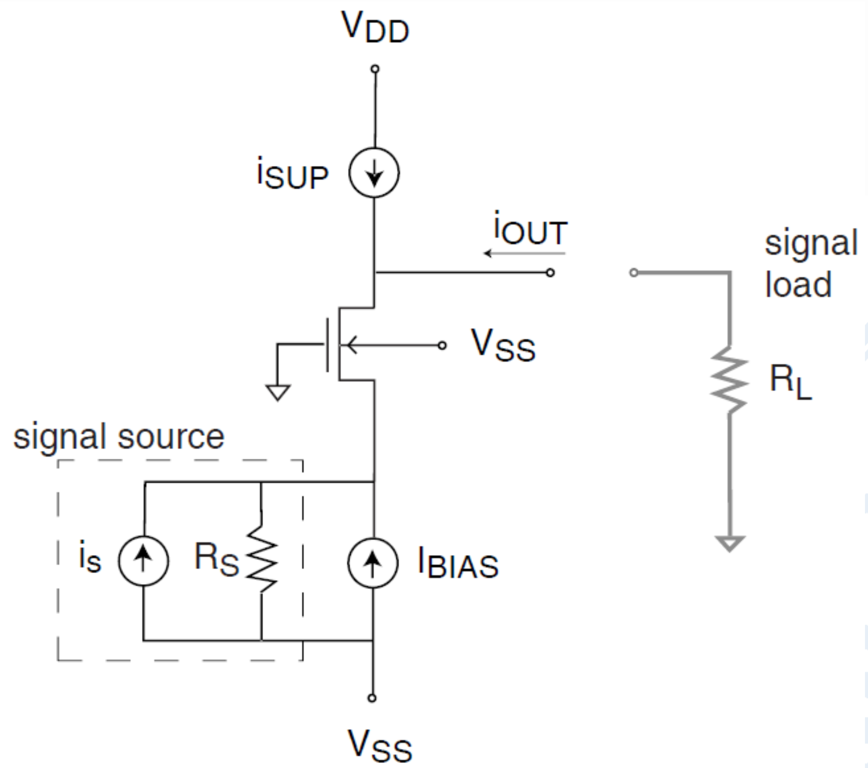
3. Common gate amplifier

Need to handle current mode signal sources:



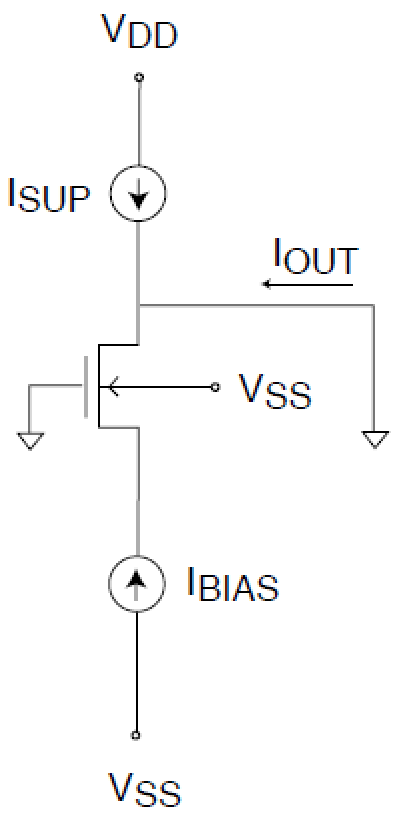
How does it work?

• Since source is signal input terminal, body cannot be tied up to source (C_{sb} is significant)

• i_{SUP}, I_{BIAS}, and W/L selected to bias MOSFET in saturation, obtain desired output bias point, and desired output swing.

• no current gain: $i_s = i_{out}$ (current buffer)

- Bias: select I_{SUP}, I_{BIAS}, and W/L to get proper quiescent I_{OUT} and keep MOSFET in saturation



$$I_{SUP} + I_{OUT} + I_{BIAS} = 0$$

Select bias so that I_{OUT}=0=> V_{OUT}=0.

Assume MOSFET in saturation (no channel modulation):

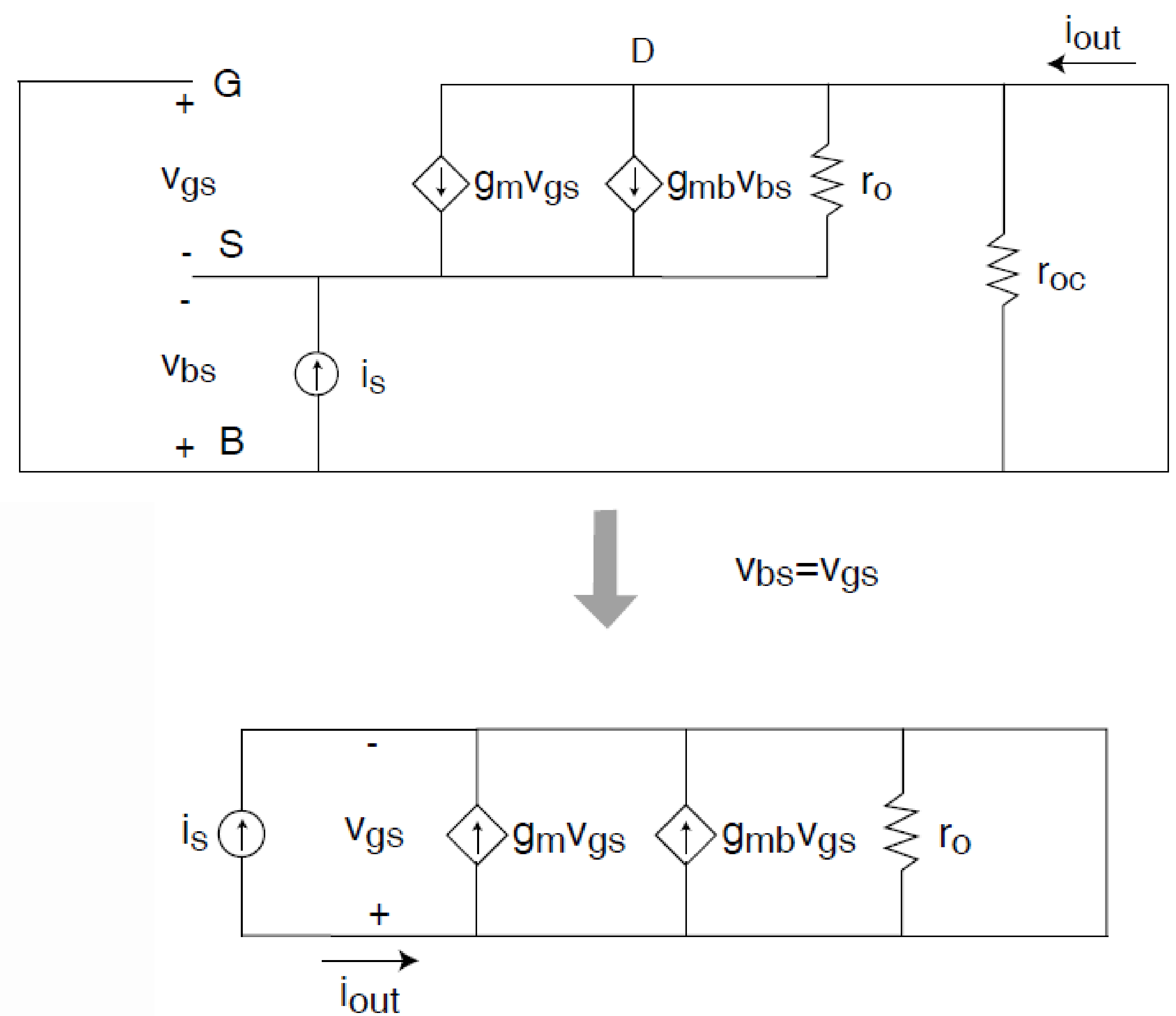
$$I_D = \frac{W}{2L}\mu_n C_{ox}(V_{GS} - V_T)^2 = I_{SUP} = -I_{BIAS}$$

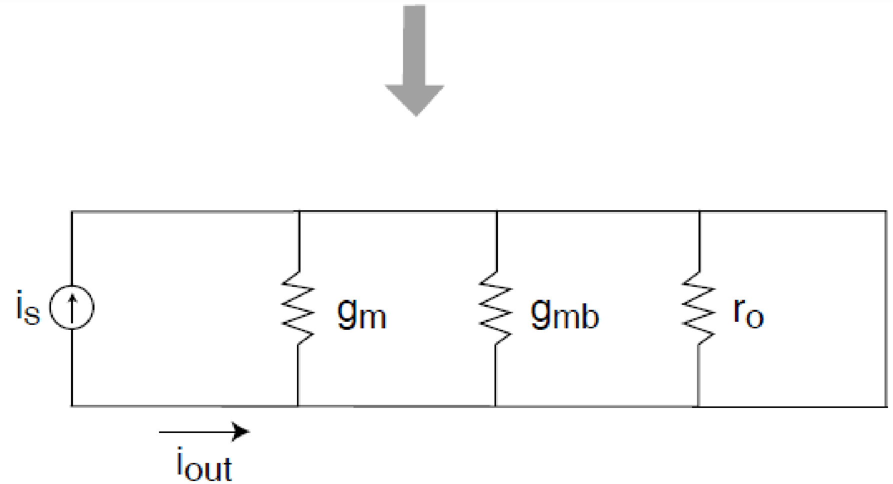
but V_T depends on V_{BS}:

$$V_T = V_{To} + \gamma_n(\sqrt{-2\phi_p - V_{BS}} - \sqrt{-2\phi_p})$$

Must solve these two equations iteratively to get V_S.

☐ Small signal circuit (unloaded)

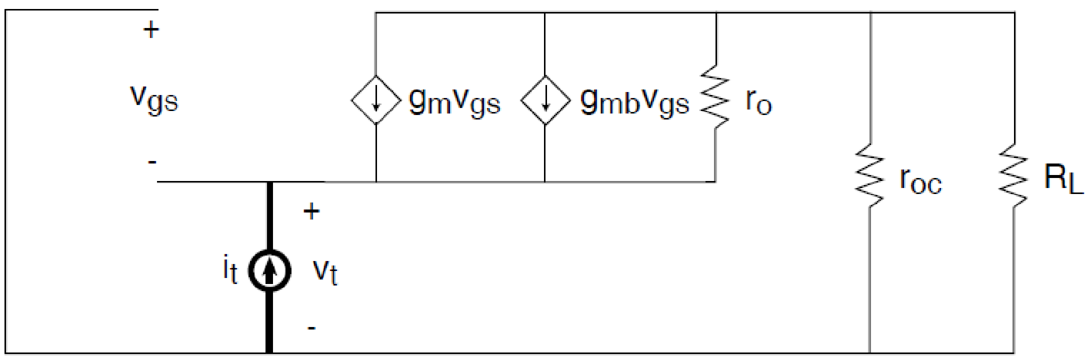


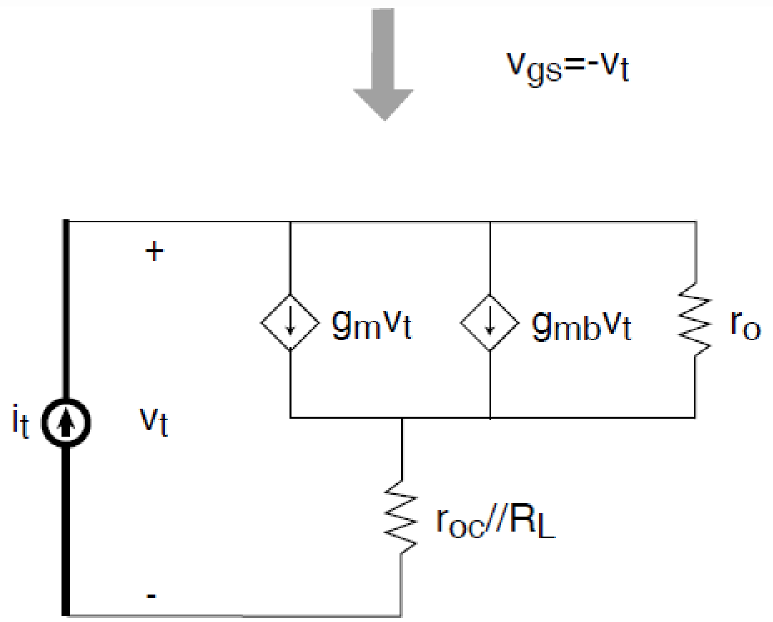


$$i_s = -i_{out} \Rightarrow A_{io} = -\frac{i_{out}}{i_s} = -1$$

Not surprising, since in a MOSFET: $i_g = 0$.

Input resistance:





Do KCL on input node:

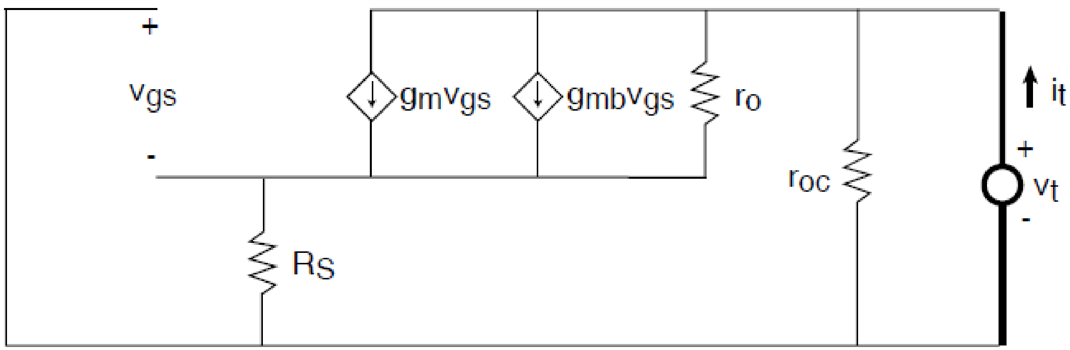
$$i_t - g_m v_t - g_{mb} v_t - \frac{v_t - (r_{OC} // R_L) i_t}{r_o} = 0$$

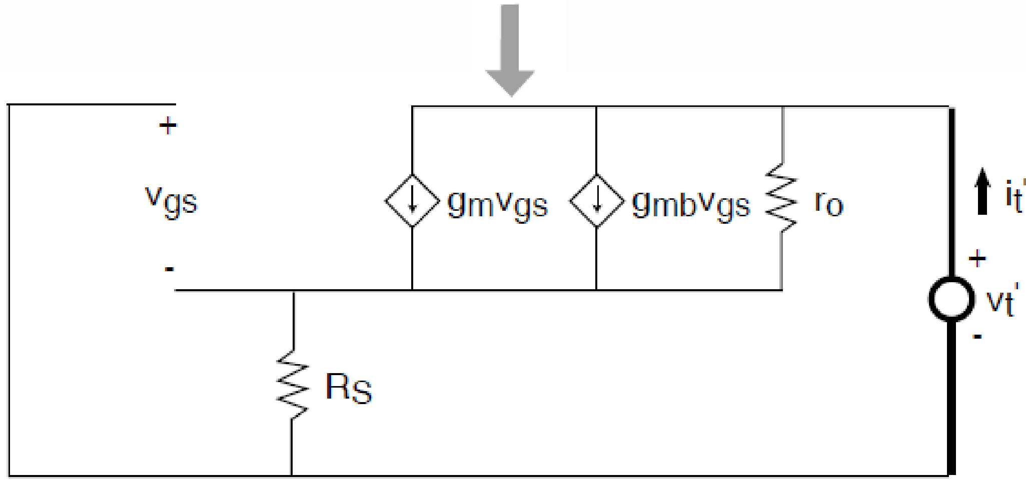
Then:

$$R_{in} = \frac{1 + \frac{r_{OC} // R_L}{r_O}}{g_m + g_{mb} + \frac{1}{r_O}} \approx \frac{1}{g_m + g_{mb}}$$

Very small.

Output resistance:





Do KCL on output node:

$$i_t' - g_m v_{gs} - g_{mb} v_{gs} - \frac{v_t' + v_{gs}}{r_O} = 0$$

Notice also:

$$v_{gs} = -i_t' R_S$$

Then:

$$R_{out} = r_{OC} // \left\{ r_O \left[1 + R_S \left(g_m + g_{mb} + \frac{1}{r_O} \right) \right] \right\} \approx r_{OC} // \left[r_O (1 + g_m R_S) \right]$$

Very large, because of the feedback effect of R_S.

Summary of MOSFET amplifier stages:

stage	A_{vo}, G_{mo}, A_{io}	R_{in}	R_{out}	key function
common source	$G_{mo} = g_m$	∞	$r_o // r_{oc}$	transconductance amp.
common drain	$A_{vo} \simeq \frac{g_m}{g_m + g_{mb}}$	∞	$\frac{1}{g_m + g_{mb}}$	voltage buffer
common gate	$A_{io} \simeq -1$	$\frac{1}{g_m + g_{mb}}$	$r_{oc} // [r_o(1 + g_m R_S)]$	current buffer

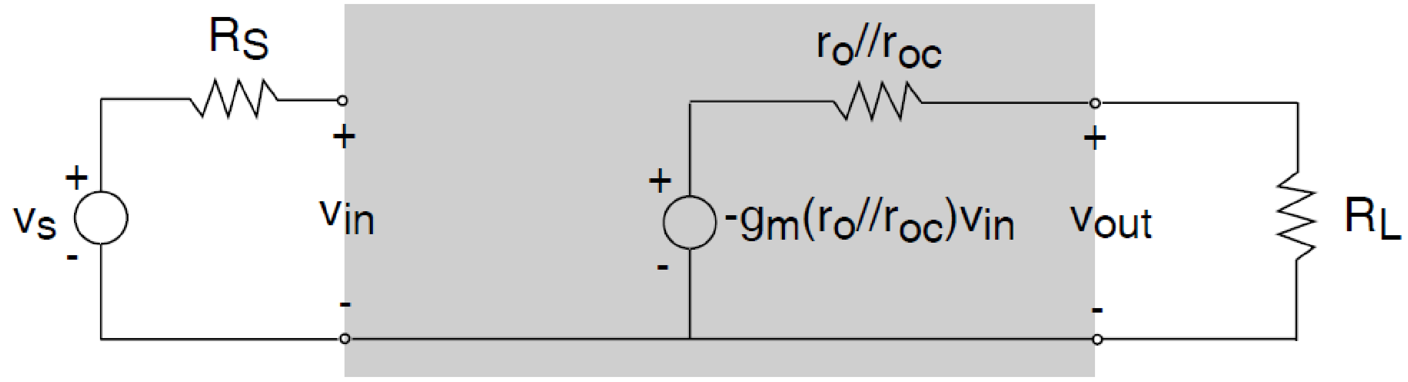
In order to design amplifiers with suitable performance, need to combine these stages

$\Rightarrow$ multistage amplifiers

CMOS multistage voltage amplifier

Goals:

- high voltage gain
- high R_{in}
- low R_{out}
- Good starting point: CS stage

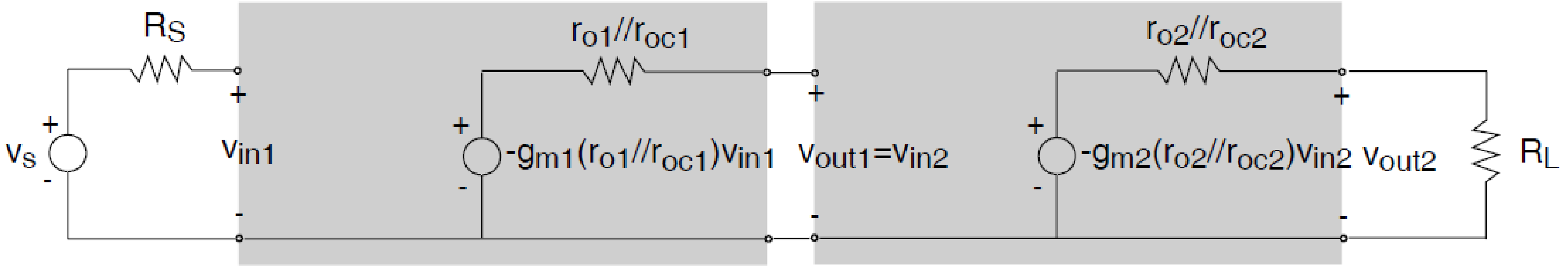


$$R_{in} = \infty$$

$$A_{vo} = -g_m(r_O // r_{OC}), \textit{probably insufficient}$$

$$R_{out} = r_O // r_{OC}, \textit{too high}$$

Add second CS stage to get more gain:

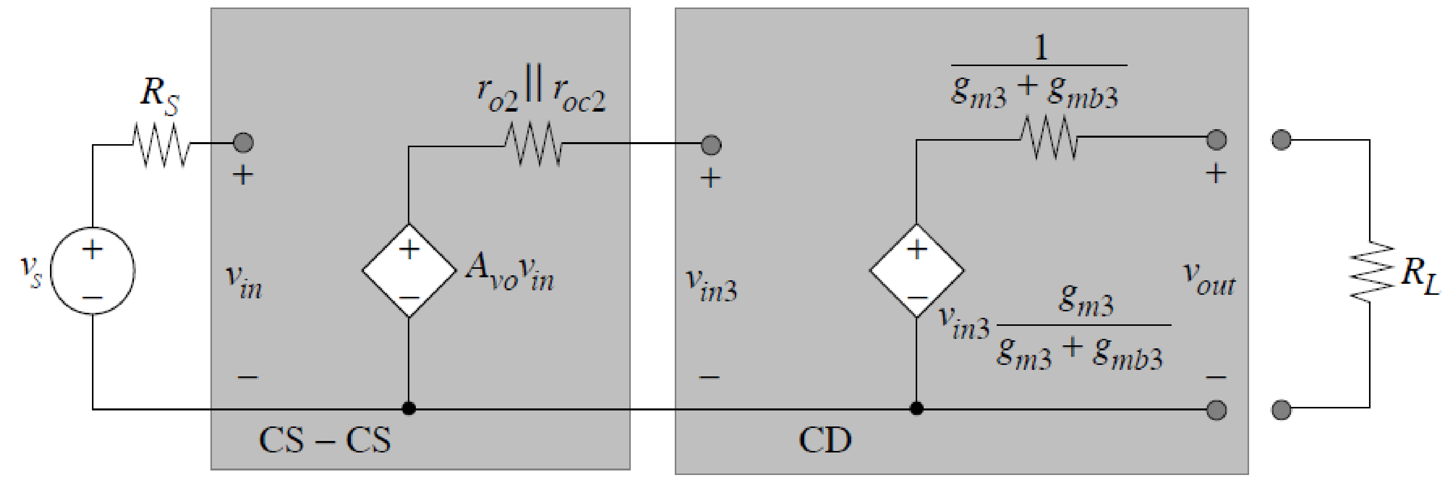


$$R_{in} = \infty$$

$$A_{vo} = g_{m1}(r_{O1} // r_{OC1}) g_{m2}(r_{O2} // r_{OC2})$$

$$But\, R_{out} = r_{O2} // r_{OC2}, still\ high$$

Add CD stage at output:



$$R_{in} = \infty$$

$$A_{vo} = g_{m1}(r_{O1}//r_{OC1})g_{m2}(r_{O2}//r_{OC2})\frac{g_{m3}}{g_{m3}+g_{mb3}}, \text{ still high}$$

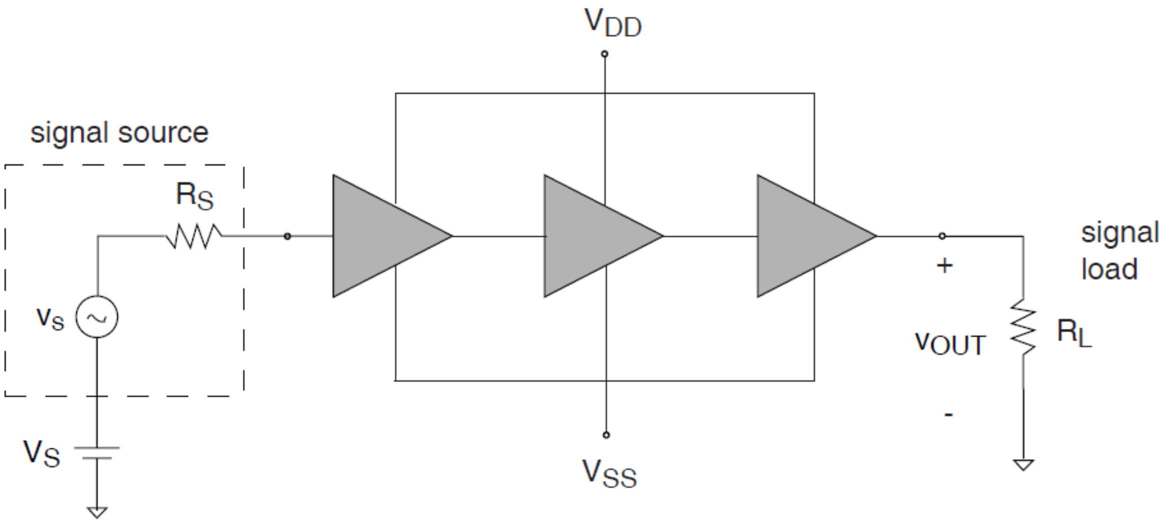
$$R_{out} = \frac{1}{g_{m3}+g_{mb3}}, \text{now small}$$

◆ Amplifier requirements are often demanding:

- must adapt to specific kinds of signal source and load,
- must deliver sufficient gain

◆ Single-transistor amplifier stages are very limited in what they can accomplish

⇒ multistage amplifier.



Key conclusions

Different MOSFET stages designed to accomplish different goals:

- Common-source stage:

  large voltage gain and transconductance, high input resistance, large output resistance

  excellent transconductance amplifier, reasonable voltage amplifier

- Common-drain stage:

  no voltage gain, but high input resistance and low output resistance

  good voltage buffer

- Common-gate stage:

  no current gain, but low input resistance and high output resistance

  good current buffer