上海交通大学
SHANGHAI JIAO TONG UNIVERSITY

Lecture 2

VLSI Fabrication Technology

Contents

- IC technologies
- IC fabrication step
- CMOS devices
- VLSI layout

IC technologies

- Before 1980s, the bipolar technology.
- After 1980s, CMOS technology dominated, leaving the bipolar technology to fill specialized function such as high-speed analog and RF circuits.
- BICMOS incorporates CMOS and bipolar technology, providing the best of both technologies. But it is costly and CMOS continues to improve itself.
- CMOS processes can be identified as n-well, p-well, and twin-well processes.
- Other technologies:

  Gallium arsenic (GaAs) for RF and optical devices.

IC FABRICATION STEP

8 steps

1. **Wafer （原片） preparation**
2. **Oxidation （氧化）**
3. **Diffusion （扩散）**
4. **Ion implantation （离子注入）**
5. **Chemical vapor deposition (CVD) （化学气相沉积）**
6. **Metallization （金属化）**
7. **Photolithography （光刻）**
8. **Packaging （封装）**

some of these steps may be carried out several times

1. Wafer Preparation

1.The material is grown as a single **crystal ingot** （晶体锭） and then sawed to produce wafers 10 to 30 *cm* in diameter and 400 to 600 μm thick.

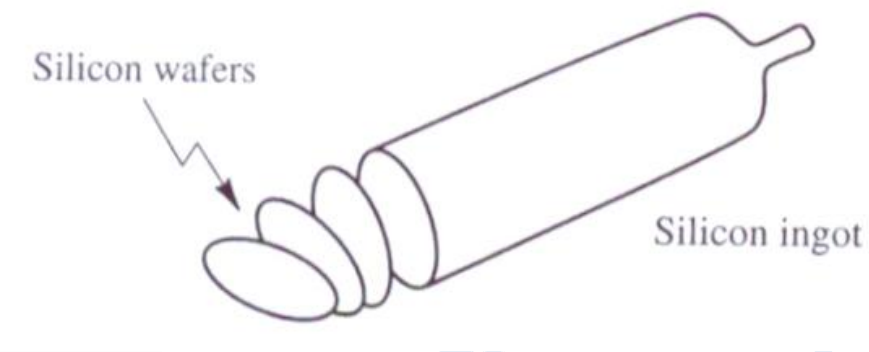


Fig Silicon ingot and wafer slices

2. The surface of the wafer is then polished to a mirror finish using chemical and mechanical polishing (CMP) techniques.

3. Foundry （晶圆代工厂） provides **wafer** to semiconductor manufacturers.

2. Oxidation

- It refers to the chemical process of silicon reacting with oxygen to **form silicon dioxide**, SiO_2.

$$Si + O_2 = SiO_2$$

- The process can be classified as two types:

Dry oxide （干法氧化）: Introduce high-purity gas.

It gives electrical characteristics.

Wet oxide （湿法氧化）: Introduce water vapor.

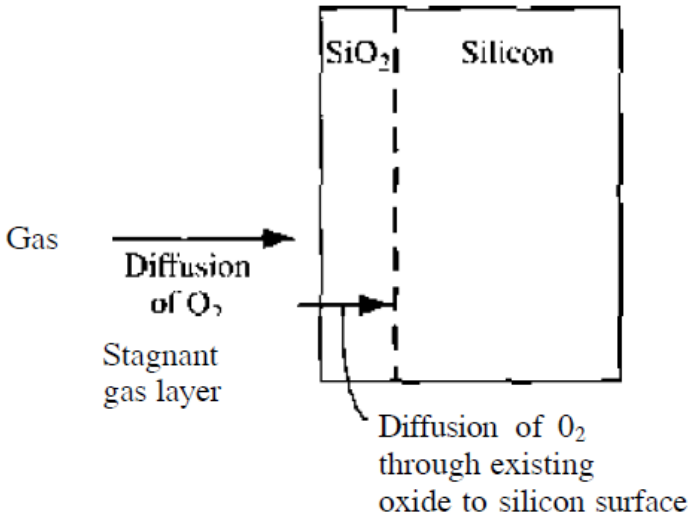


Fig Schematic of the Oxidation Process

SiO_2 is used to form

- **insulator**
- **capacitor** （电容）
- an effective **mask** （掩膜）
  against many impurities in SiO_2 region,
  but allowing the introduction of dopants into Si region.

3. Diffusion

- It **introduces impurity atoms** (dopants) into silicon to change its resistivity （电阻率）.
- **Dopant types:**
  - —p-type dopants: boron （硼）.
  - —n-type dopants: phosphorus （磷） and arsenic （砷）.
- **A PN junction**
  - — formed by diffusing p-type dopants into an n-type substrate （衬底）.

4. Ion Implantation

- An alternative process to **replace diffusion**

  --used to introduce impurities into silicon.

- An ion implanter

  —produces ions of the desired impurity

  —accelerates them by an electric field,

  —allows them to strike the silicon surface.

- It is used for **accurate control** of the dopants.

5. Chemical Vapor Deposition (CVD)

- An alternative process to **replace oxidation**
  - gases or vapors are chemically reacted, leading to the formation of a solid on a substrate.
  - a fast process at a low temperature.
- Used to deposit silicon dioxide （SiO_2） on a silicon substrate.
  - not as good as oxidation
  - good enough to act as an **electrical insulator**.

6. Metallization

- The purpose of metallization is to **interconnec**t the various components of the IC to form the desired circuits.
- Process
  - The **aluminum (铝)** is deposited by heating it until it vaporizes
  - The vapors contact the silicon surface and condense to form a solid aluminum layer.
  - Finally the required interconnection pattern is selectively **etched** （刻蚀）.

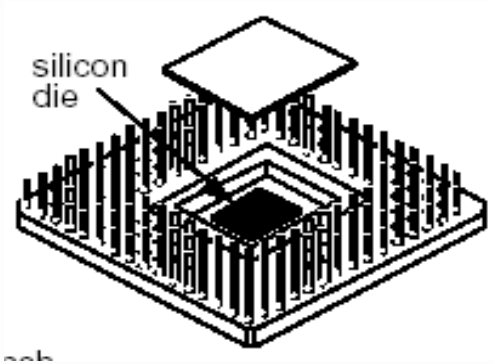
7. Photolithography

- The surface geometry of the various integrated-circuit components is defined by Photolithography
- Process:
  - Coating the silicon surface with a photosensitive（光敏）layer called photoresists （光刻胶）
  - Exposing the surface to light through a master pattern （掩膜）on a photographic plate
  - Removing the softened photoresist using a chemical developer, causing the mask pattern to appear on the wafer

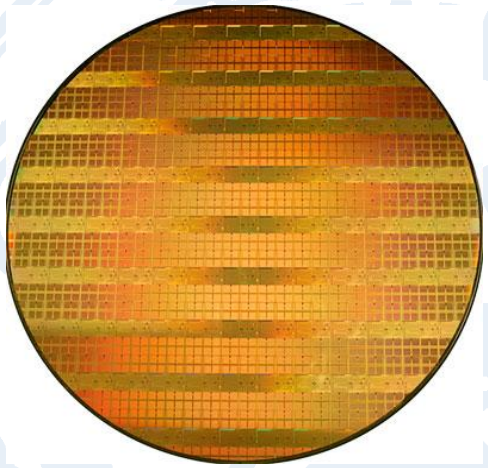
8. Packaging

- A finished wafer contains more than several hundreds of chips.
  - Each chip may contain 10-10^9 transistors.
  - The size of a chip is between 1 and 10 *mm* on each side.
- Then chips are separated from each other by dicing.

• Chips are mounted in packages.

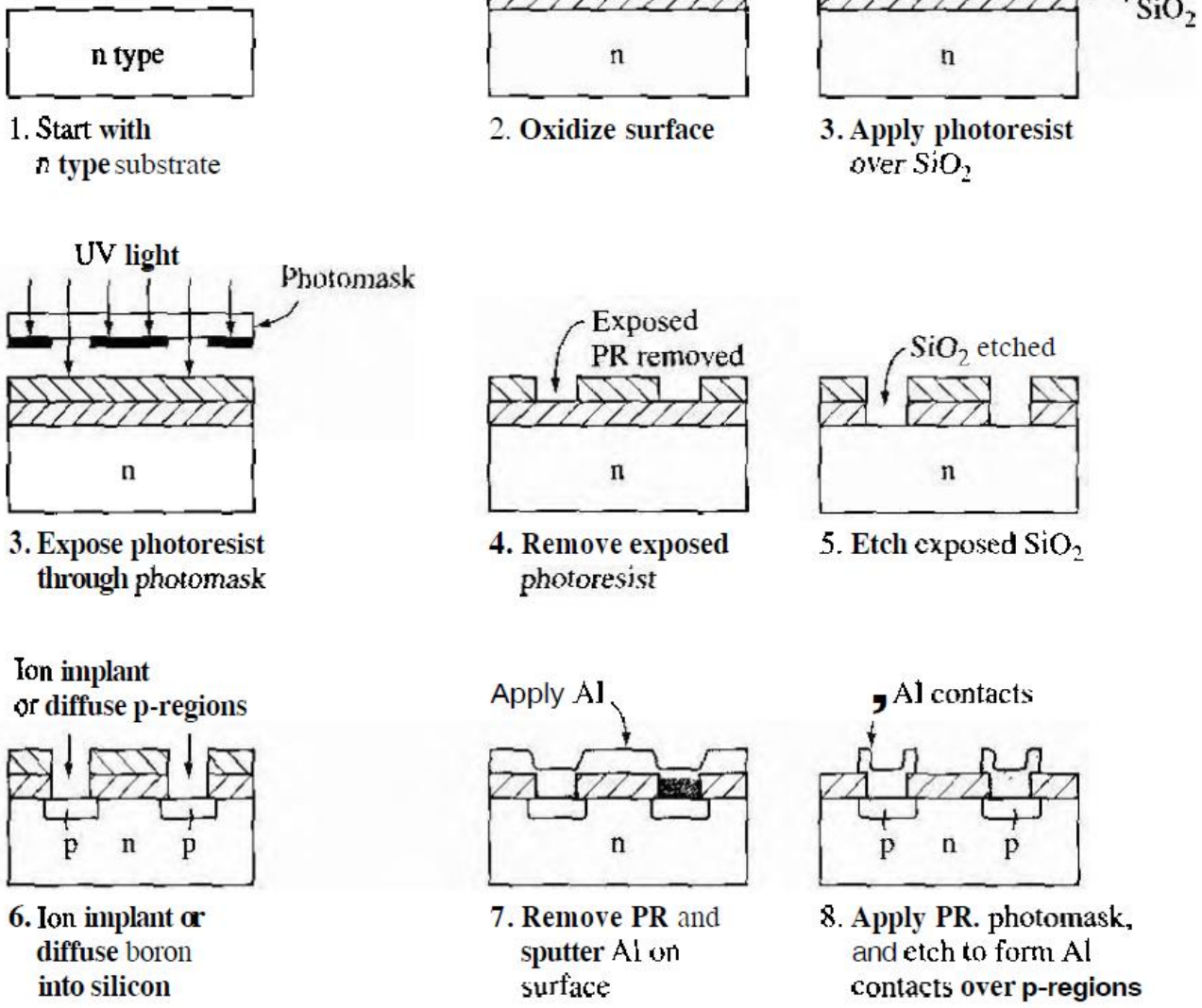


Packaging

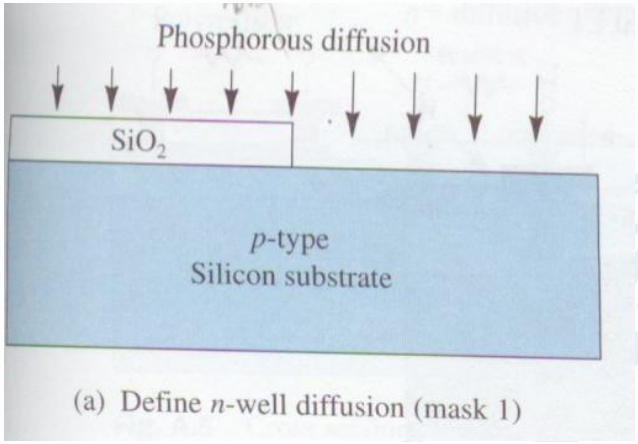


Wafer

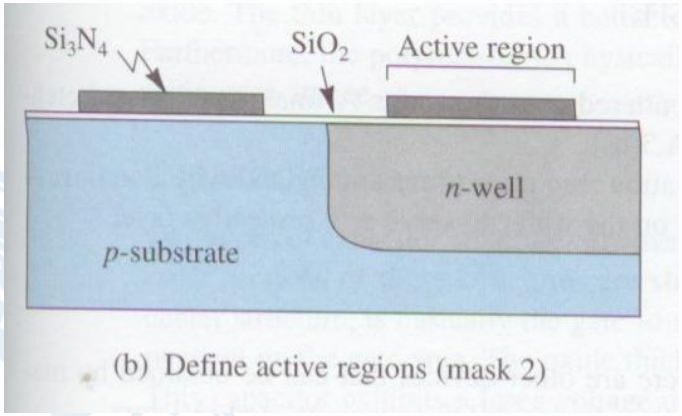
The steps to form PN junctions



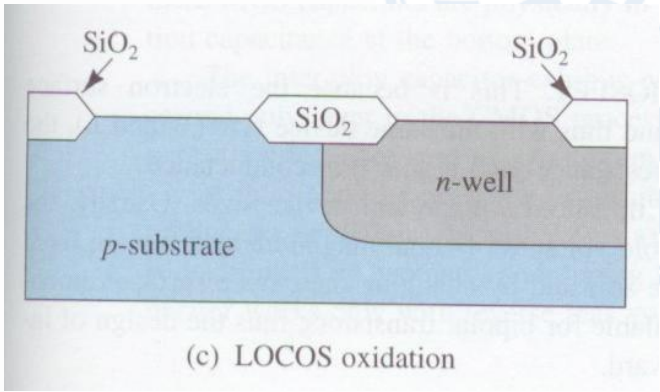
n-well CMOS process



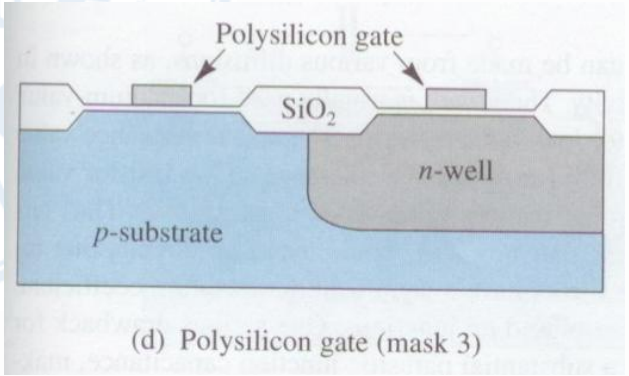
n-well （井）: is formed by phosphorous diffusion.



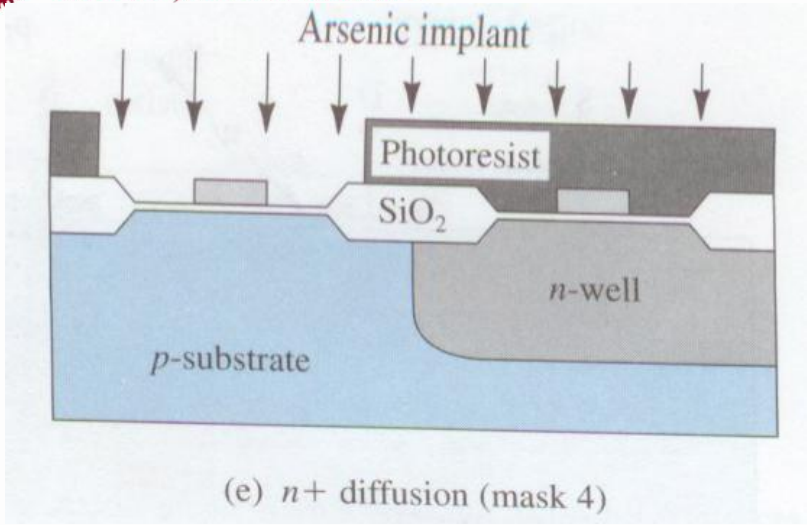
Active region: n+ diffusion by arsenic implant; p+ diffusion by boron implant.



SiO2: by local oxidation

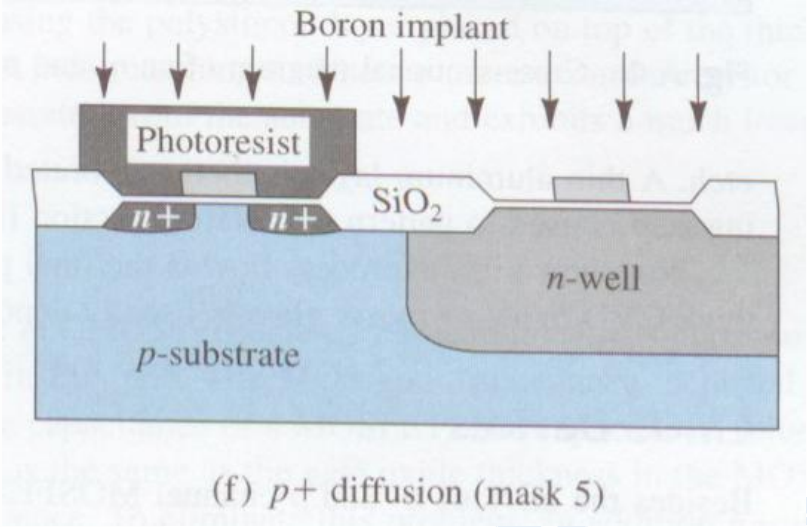


Polysilicon gate: is deposited by arsenic doped and patterned by mask.



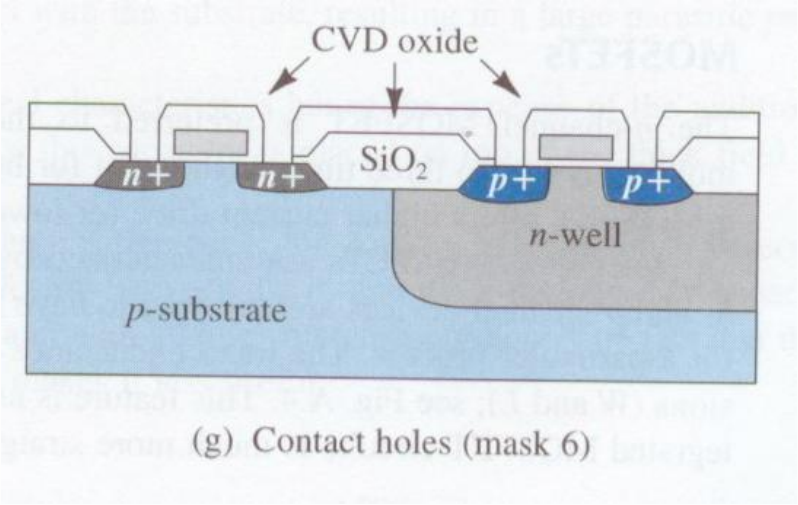
(e) $n+$ diffusion (mask 4)

To form NMOS



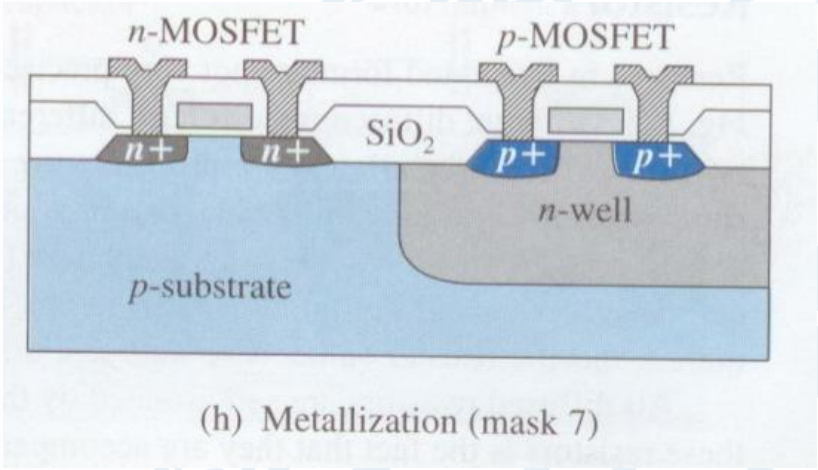
(f) $p+$ diffusion (mask 5)

To form PMOS



(g) Contact holes (mask 6)

Layer insulator: CVD oxide



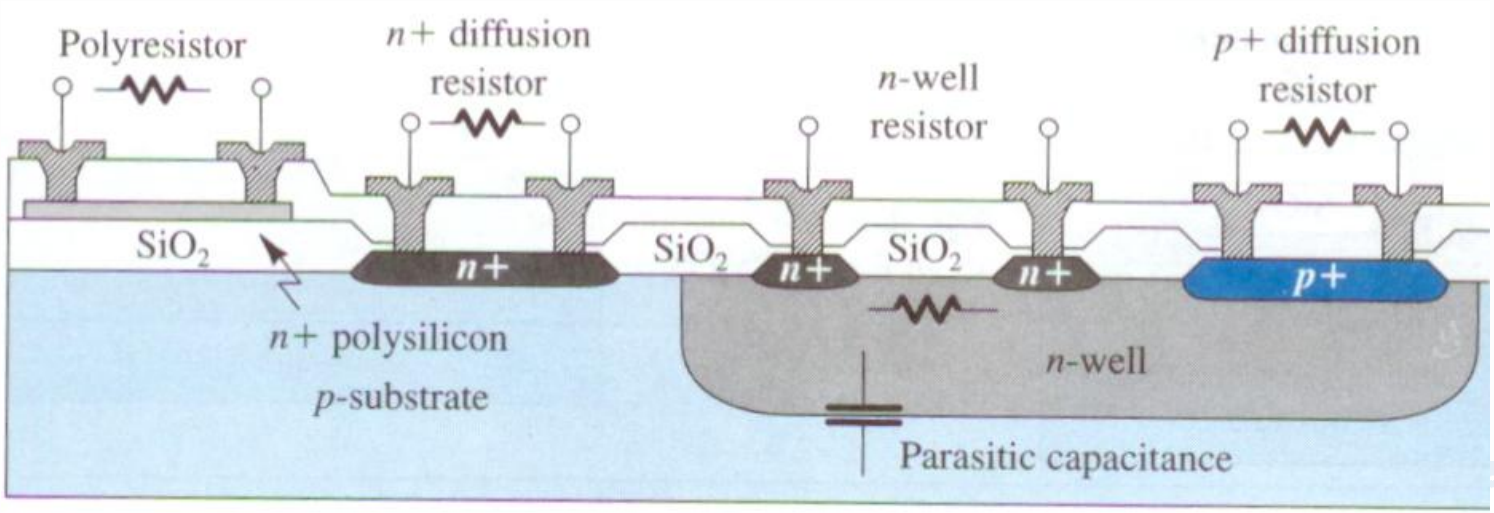
(h) Metallization (mask 7)

Contact: by metallization.

CMOS devices

- Resistors
- Capacitors
- PN-junction diodes
- Inverters

Resistors



- **Resistor fabricated using well and diffusion**

---n+ diffusion resistor, n-well resistor, p+ diffusion resistor

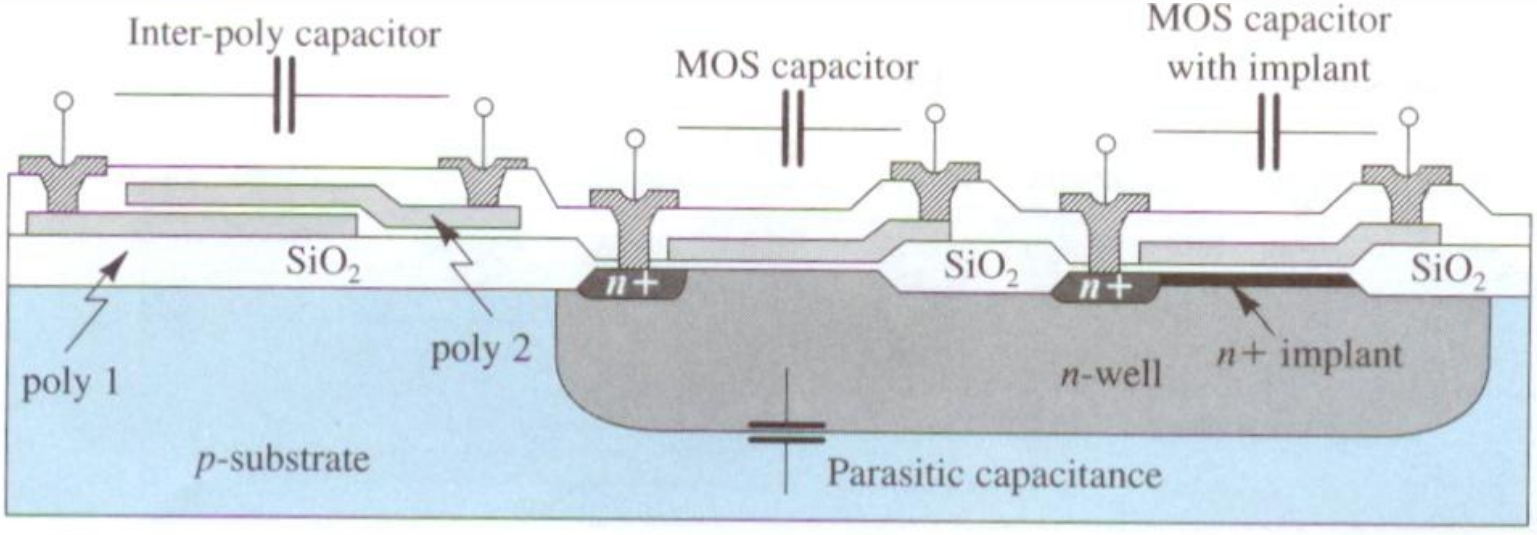
--- accompanied by a parasitic junction capacitance, making them not very useful for high-frequency application.

- **Resistor fabricated using polysilicon layer**

--- polyresistor

--- better performance.

Capacitors

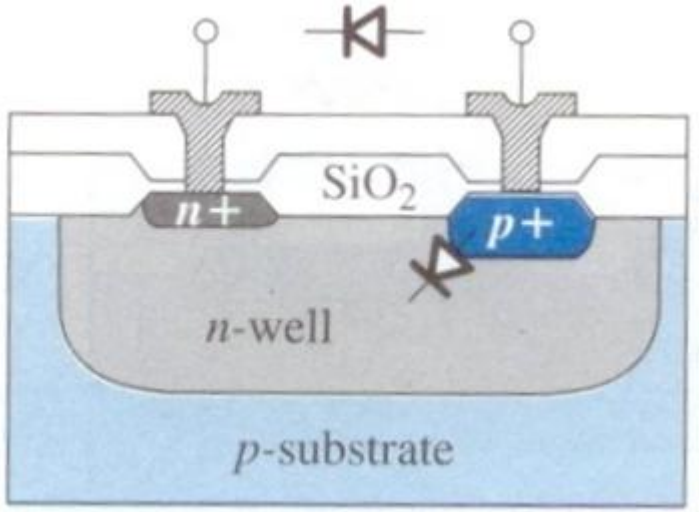


- **a) Inter-poly capacitor**: poly1-poly2 capacitor
  --- exhibits near ideal characteristics
  --- at the expense of the addition of a second ploy layer.
- **b) MOS capacitor**: the gate-to-source capacitance
  --- voltage dependent.
- **c) MOS capacitor with implant**:
  --- to eliminate voltage dependence of MOS capacitor.

Both b) and c) include a large parasitic pn junction capacitance at the bottom plate.

PN-junction diodes

PN junction diodes



PN-junction diodes

--- using n-well process to provide a high breakdown voltage.

--- its forward voltage drop varying with temperature

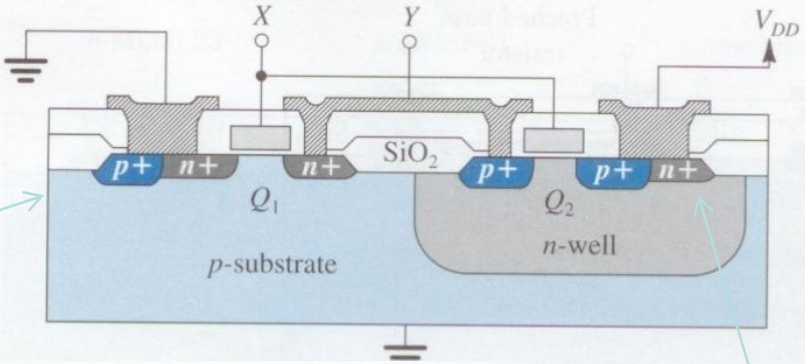
The application:

--- **the input clamping circuits（钳位电路）** for protection against electrostatic discharge.

--- **on-chip temperature sensor （温度传感器）** by monitoring the variation of its forward voltage drop.

Inverters

Substrate tie, connect to ground to avoid latchup （闩锁）.



Well tie